IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INTEL CORPORATION,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 00-796-RRM
	)	
BROADCOM CORPORATION,	)	
	)	
Defendant.	)	

MEMORANDUM OPINION

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Wilmington, Delaware
November 6, 2001

McKELVIE, District Judge

This is a patent case. Plaintiff Intel Corporation is a Delaware corporation with its principal place of business in Santa Clara, California. Intel owns U.S. Patent Nos. 4,823,201 (the ’201 patent); 4,975,830 (the ’830 patent); 5,894,410 (the ’410 patent); 5,079,630 (the ’630 patent); and 5,134,478 (the ’478 patent). Defendant Broadcom Corporation is a California corporation with its principal place of business in Irvine, California.

On August 30, 2000, Intel filed its complaint in this case alleging that Broadcom is infringing, inducing infringement, or committing acts of contributory infringement of one or more claims of the ’201 patent, the ’830 patent, the ’410 patent, the ’630 patent, and the ’478 patent.

On October 10, 2000, Broadcom moved to dismiss Intel’s complaint or, in the alternative, to transfer the action to the United States District Court for the Northern District of California. After eleven months of discovery, the court heard oral argument on Broadcom’s motion on September 24, 2001. In a memorandum opinion dated October 9, 2001, the court denied Broadcom’s motion.

On September 24, 2001 hearing, the court also heard oral argument in accordance with Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996), to construe the claims of the five patents. The claim construction issues for each of the five patents are now fully briefed by the parties.

In order to simplify the issues before the jury and to shorten the length of the jury trial, the court required that the trial proceed in two parts. The first trial will be a three week jury trial on the ’201and the ’830 patents. A subsequent trial will cover the remaining three of the five patents.

This is the second of two memorandum opinions that will set forth the court’s claim construction of asserted claims of the ’201 and ’830 patents. This opinion will consider the two asserted claims of ’201 patent, claims 1 and 10.

I. FACTUAL AND PROCEDURAL BACKGROUND

The court draws the following facts from the parties briefing, documents submitted by the parties, and from the prosecution history of the patents at issue.

A. Background of the Technology

The ’201 patent, along with the ’630 and ’478 patents (collectively referred to “the digital video patents”), generally relate to techniques for reducing digital data volume and then expanding the data back to its original state so that it can be displayed and viewed normally. These techniques are commonly referred to as compression (i.e. encoding) and decompression (i.e. decoding).

This section will provide background in this field of technology. In composing this section, the court draws heavily from Intel’s Opening Markman Brief for the ’630 Patent, in which Intel has provided an overview of the technology field of digital video compression and decompression that it has labeled a “technology tutorial.” It does not

appear that the parties dispute any of the background of the digital video field. This background section is intended to give a helpful context to the analysis of the digital video patents and should not be construed as part of the court's findings on claim construction.

1. Digital Video

As is commonly known, "video" refers to recording and displaying moving objects from the real world. For example, movies shown in a theater are produced on reels of film consisting of a long sequence of many still images, which are called frames. When the frames are run through a projector at a predefined rate (in general, 30 frames per second) and projected on a screen, the viewer experiences a sense of uninterrupted motion. Because of limitations in the speed in which they process sequences of images, the human eyes and brain do not detect that they are seeing a sequence of still images displayed in rapid succession.

Historically, motion video was produced, distributed, and used in analog form. Analog refers to a waveform signal that is continuously varying in strength or quantity, rather than based on discrete units (i.e. digital). Microsoft Computer Dictionary 22 (4th ed. 1999). Analog images, such as a photograph taken from a traditional non-digital camera, are formed from light waves, which may have infinite gradations of brightness and color.

Analog information, including images, may be represented in digital format.

Digital refers to any system based on discrete numerical values, as opposed to infinitely varying analog waves. The numerical values may be based on any number system, but most often use the binary number system. The binary number system has only two possible values – '0' and '1.' In a binary number system, each 0 or 1 is known as a bit. Using binary, bits can be combined to represent Arabic numbers, letters, words, sentences, etc. Similarly, a collection of 0s and 1s can be used to represent a still image or a motion picture.

Digitally encoded video signals contain a significant amount of redundant information. Redundancies exist within a single frame, for example, if a portion of the frame is the same color. Redundancies may also exist between consecutive frames in a sequence where all or a portion of a current frame is identical to a previous frame. One of the primary advantages of representing information in digital form is that by using a mathematical conversion (or compression) technique, the redundancies in the digital data may be reduced so that the data can be stored in less space or transmitted in less bandwidth. Different compression techniques are focused on exploiting different types of data redundancies to reduce the overall data volume that is necessary to represent the video information. Once the data is required for use, it can be decoded (or decompressed) using an inverse mathematical conversion which restores compressed data to its original form, or a close approximation thereof. Techniques relating to compression and decompression are largely responsible for bringing digital motion video to computers,

digital cable, and DVD players.

Still and moving images, whether analog or digital, are made up of many picture elements, known as “pixels,” which are the smallest element of an image. In black and white analog video, each pixel has a brightness level called luminance, which is measured along a scale from black to white to infinite shades of gray. By contrast, in black and white digital video, each pixel is assigned a discrete luminance value that commonly ranges between 0 and 255, which each value representing a particular luminance level. At one extreme, 0, the pixel would be painted black, whereas at the other extreme, 255, the pixel would be painted white, with all other pixel values 1-254 being painted various shades of gray. In this commonly implemented scheme, the pixel values may then be represented by binary numbers – specifically, values 0 through 255 correspond to binary numbers 00000000 through 11111111. Thus, in black and white digital video, pixel luminance values ranging from 0 to 255 are eight bits in length.

Color digital video also has a luminance component, but it also has two components that capture information about color called chrominance. The combination of luminance and chrominance components yields color video. As with luminance, each color (or chrominance) component is assigned a value between 0 and 255. Each pixel in color digital video, therefore, has three eight bit values associated with it, each value between 0 and 255.

Like standard film reels, digital video is made up of a sequence of digitized

frames. Each frame includes many pixels, with each pixel represented, for example, by numerical values from 0 to 255, or eight bits from 00000000 to 11111111 in binary format. In the U.S. most televisions display a format known as standard definition television, or "SD-TV." In SD-TV, each frame has up to 480 horizontal lines of pixels and up to 720 pixels per line. Thus, a single frame of SD-TV video has as many as 345,600 pixels. North American television also uses approximately 30 frames per second of video, meaning that over 10 million pixels are displayed per second. That means that SD-TV uses as much as nearly 240 million bits per second.

A new television format currently being deployed in the U.S. is known as high definition television, or "HD-TV." HD-TV, which promises a clearer more lifelike picture, achieves that result by using many more pixels horizontally and vertically than SD-TV, with up to 1080 lines of pixels and up to 1920 pixels per line. HD-TV may use over 2 million pixels in a single frame and a 30 frames per second, which translates to over 1.4 billion bits per second.

The enormous bit volume of either SD-TV or HD-TV places a heavy burden on devices used to store digital video data – such as CD-ROMs, DVDs, and computer hard disks – and on digital video transmission systems, including digital cable and satellite TV systems. As a result, various techniques for reducing data volume are used in the storage and transmission of digital video data.

2. Compression and Decompression

As noted above, compression or encoding is used to reduce digital data volume so that it can be stored in less space or transmitted using less bandwidth, whereas decompression or decoding restores compressed data to its original form or a close approximation thereof. Microsoft Computer Dictionary 102, 457 (4th ed. 1999).

There are two key measures of the success of the compression-decompression system that is to be used to encode and decode digital video data. First, a compression technique must be able to achieve an extremely high degree of compression. Intel's '630 patent is directed "to meeting the need for a compression system for providing a compressed digital video signal representative of a full motion color video signal." Col. 1:47-49.

The second important feature of a compression-decompression system that is designed to handle digital video, is that a decompression technique must be able to be applied quickly. To allow for smooth video playback without jerkiness or blocky artifacts on a computer, cable system, or DVD player, the compressed data must be decoded in "real-time." Real time computer operations must proceed at the same rate as a physical or external process; in this case, at the same rate that video is displayed and watched, i.e. 30 frames per second. Id. at 375.

B. The Patented Technology

The invention of the ’201 patent is a single-chip integrated circuit that enables the decompression of compressed full motion video data in real time. To understand how the ’201 patent decompresses compressed data, it is first necessary to understand some of the principles behind the different types of video compression techniques.

1. Relevant Encoding and Decoding Techniques

One class of techniques that are designed to reduce redundancies within a single frame is called absolute (or intra-frame) encoding. Assume that a frame shows a balloon drifting across a blue sky. In this example, the color of a ten pixel block that is part of the background sky is completely uniform. An absolute encoding technique exploits this redundancy by indicating that a certain number of pixels all have the same digital value. In a black and white digital system, instead of transmitting the 8-bit luminance value for each of the ten pixels (80 bits), one can encode the consecutive pixels by simply sending one 8-bit luminance value and a short ten bit code saying “repeat that pixel value 9 more times.” Instead of sending 80 bits, the encoder can send the information about those ten pixels using 18 total bits. The encoder processes the data, determines the redundancy, and send the 18 bits to a decoder, which displays the 8 bit pixel once, and then sends the 10-bit re-display code. The decoder recognizes this code as meaning re-display the same pixel 9 times, and performs this operation, as instructed.

A second class of techniques that is used to reduce redundancies that exist between

two consecutive frames is called relative (or inter-frame) encoding. Given that each frame represents 1/30 of a second, the content of consecutive frames is often very similar. In the example of the balloon drifting across the sky, the only difference between certain blocks of pixels that represent the blue sky in the two consecutive frames is that the color of the sky in the current frame is slightly different. Instead of transmitting all of the bits associated with each block of pixels in a frame, relative encoding techniques are used to capture information about the differences between the previous frame and the current frame. To generate this difference information, the encoder compares the two frames and creates a difference image, which only represents the differences in the relative pixel values. The encoder first sends to the decoder an intra-frame encoded version of the first frame. Then, instead of transmitting the next frame, the encoder can transmit information, in the form of a few bits of code, to the decoder that tells the decoder how to construct the current frame using the previous frame, which the decoder already has, and the difference information. When the current frame and previous frame are similar, this technique requires fewer bits than transmission of both frames, because the digital values of the difference image are typically small numbers, which require fewer bits to transmit.

Relative encoding also involves another similar principle known as motion compensation. Again referring to the example of the balloon drifting across the sky, one of the only differences between two consecutive frames is that the balloon in the current frame has moved, or shifted slightly, to a different location. Much of the background

information is redundant. In order to encode for motion compensation, the encoder seeks to determine the motion of the balloon by selecting a block of pixels corresponding to the balloon in the current frame, or a portion of the balloon, and searching the previous frame to find a block of identical, or closely matching pixels. Once it finds a match, the encoder determines how far and in what direction, the block of pixels in the current frame has moved with respect to the block in the previous frame. In this way, the encoder generates a motion vector or displacement vector, which represents the direction and magnitude of motion of the current frame relative to the matching previous frame block. This vector, simply stated, represents the number of pixels the balloon has moved across the frame.

Once the encoder determines the motion vector, it applies the motion vector to a reconstructed version of the previous frame, to obtain a prediction of the block in the current frame. Because both the encoder and decoder keep a copy of the reconstructed previous frame, they operate on the same image when applying the motion vector. The encoder uses the predicted block from the reconstructed previous frame to generate a difference image. The encoder sends the motion vector and the difference image to the decoder. The difference image is typically encoded using absolute encoding, and the motion vector may be encoded in the same fashion. The decoder uses the decoded motion vector to obtain the predicted block from the decoder's copy of the reconstructed previous frame. Finally, the decoder adds the pixel values in the decoded difference image to obtain the block that will be displayed in the current frame.

Again, motion compensation encoding techniques applied in this manner achieves compression because the encoder need transmit only the encoded difference image and motion vector to the decoder, rather than the current frame. Generally, the encoded error image and motion vector are represented in fewer bits than an absolute encoding block of the current frame.

2. The ’201 Patent

As noted above, the ’201 patent relates to a high-speed, single chip video processor that receives an encoded (i.e. compressed) video signal and rapidly decodes that signal to generate an uncompressed full motion video output signal that can be displayed on a television or computer monitor. The video processor includes a statistical decoder, a pixel interpolator, and arithmetic logic circuitry, all of which are controlled by a sequencer.

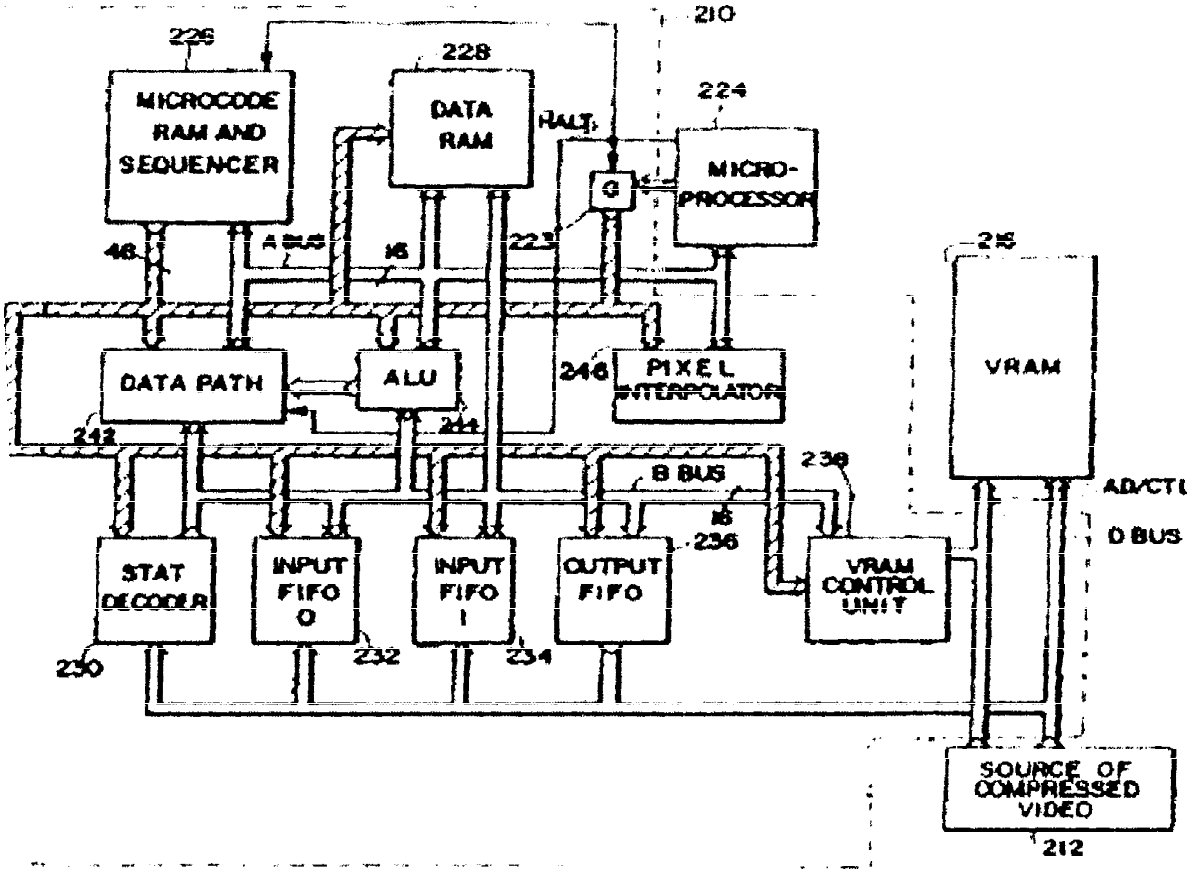
The statistical decoder decompresses information that has been compressed using statistical encoding. Statistical encoding is an encoding technique that involves assigning short bit strings for data that occurs frequently, and long codes for data that occurs infrequently. For example, if 8 bit pixels are used, there can be 256 unique pixel values. A unique variable-length-code (“VLC”) is assigned to represent each of the 256 pixel values according to their statistics – the higher the frequency of occurrence of a particular pixel value, the shorter the code, and vice versa. The statistical decoder receives the VLCs and translates them back into the original 8-bit pixel values.

The pixel interpolator of the ’201 patent is used in the decoding of inter-frame coded images. As discussed inter-frame coding is performed by searching a previous image for a matching region, encoding the location of that region as a motion vector, and encoding a difference image for the region. Sometimes, however, a matching pixel region is not found on a pixel border. Instead, the best match may be found between adjacent columns or rows of pixels. In such instances, the decoding processor must provide the previously decoded pixel values designated by a motion vector (called an “offset” in the ’201 patent) to the pixel interpolator for interpolation. Operating on the pixels from the previously decoded image, the pixel interpolator generates “interpolated pixel values” that approximate pixel values between the pixel values from the previously decoded image retrieved from memory. For a large block of pixels, interpolation is performed successively to obtain a block of “interstitial” pixel values.

The arithmetic logic circuitry performs arithmetic operations (such as addition) or logical operations (such as AND or OR). For example, during inter-frame encoding, arithmetic logic circuitry may be used to add interpolated pixel values from the previously decoded video image to error data from the current video image.

The sequencer conditions the statistical decoder, pixel interpolator, and arithmetic logic circuitry to operate simultaneously to produce decoded and decompressed pixel data. As compared with each element performing its function in serial, simultaneous operation allows the decoding process to be performed faster.

The following diagram is a simplified version of the disclosed video signal processor that is taken from Figure 2 of the ’830 patent. The elements discussed above can be seen in the diagram. The next few paragraphs will describe how the elements in the diagram interrelate to comprise a video signal processing system that embodies the invention of the ’830 patent.



As described in the patent specification, the circuitry set forth above operates as follows. Compressed video signals are provided to the video signal processing system

from a source of compressed video, that is labeled in Figure 2 of the patent (and in the above Figure) with the number 212. This source can be a CD-ROM, a DVD, etc. The compressed video signals are stored in the Video Random Access Memory (VRAM 216), which, as indicated by the dashed line, is located off of the video processing chip. The VRAM stores compressed data that is received from the source. It also stores decoded pixel data from the previous image that has been decoded. The compressed data and decoded pixel data are sent along a data bus to the statistical decoder (Stat Decoder 230) and to the input FIFO's (232 and 234). The term FIFO means first in first out. FIFO's are data storage elements in which data is removed in the same order in which it is received (i.e. in a first in, first out fashion).

The statistical decoder receives statistically encoded data and decodes it. This decoded data may be provided to the arithmetic and logic unit (ALU 244) for further processing.

The input FIFO's receive compressed data that is not statistically encoded and decoded pixel data. The input FIFO's may provide this data to the ALU for further processing. The input FIFO's may alternatively send the compressed data and decoded pixel data to the Data RAM (228), which provides temporary storage. Decoded pixel data is provided to the pixel interpolator (246) for "pixel interpolation," which generates interstitial pixel values that are used to describe the encoded image.

Interpolated pixel values are applied to the ALU together with the values provided

by the statistical decoder for further processing that adds the interpolated pixels to the difference data. The result of the ALU's operations, the decoded pixels for display, may then be routed to the output FIFO. This decoded data from the output FIFO is stored in the VRAM, which is then accessed by a display processor (not shown) that displays the decompressed video signal.

The central control element in the above described circuitry is the Microcode RAM and Sequencer (226). This circuit element controls the timing and operation of the other blocks, including the pixel interpolator, the statistical decoder, and the ALU.

Another element whose purpose is coordination is the VRAM control unit (238). The VRAM control unit coordinates data access request to the VRAM (216) from the compressed data source (212), the display processor, and the other on-chip circuitry to ensure that all of the data provided by the data source is written into the VRAM. To do so, it generates address and control signals for the off-chip VRAM.

C. Relevant Procedural History of the '201 Patent

The '201 patent issued from an application that was first filed on November 16, 1987. In that application, claims 1 and 9 correspond to the issued claims 1 and 10. On January 19, 1988, before any action had been taken by the Patent Examiner, the applicants submitted a preliminary amendment, which amended language in certain of the claims and added a new claim dependent on claim 6, which later issued as claim 7. Claim 9,

which issued as claim 10, was amended as follows:[1]

> 9. An integrated circuit for processing compressed video signal, segments of which having been encoded using different encoding processes, to provide decompressed video signal representing moving images, said integrated circuit comprising:
>
> an I/O port for coupling said integrated circuit to memory means;
>
> an address output port for coupling address signals to said memory means;
>
> a statistical decoder coupled to said I/O port for decoding variable-length- encoded compressed video signals;
>
> I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for [providing] accepting a processed video signal from said I/O port;
>
> a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal;
>
> arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values;
>
> means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O [means] circuitry, said pixel interpolator and said arithmetic processing means;
>
> control means for generating said control signals and

[1]Text that is underlined is text that was added in the Jan. 19, 1988, amendment, while text that is enclosed in brackets refers to pre-amendment language that was removed in the amendment.

> said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port; and
>
> address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means.

The Examiner did not issue an office action in response to the application. On July 21, 1988, the Examiner issued a Notice of Allowance, allowing claims 1 and 10 to issue without rejection. The '201 patent issued on April 18, 1989.

II. DISCUSSION

A. Principles of Claim Construction

1. General Principals

Patent claim interpretation is an issue that lies exclusively within the province of the court. Markman, 517 U.S. at 372. "In interpreting the claims of a patent, the court first looks to the intrinsic evidence of record, including the claims of the patent, the written description, and the prosecution history." Phillips Petroleum Co. v. Huntsman Polymers Corp., 157 F.3d 866, 870 (Fed. Cir. 1998). Construction of the claims always begins with the language of the claims themselves. See Bell Comm. Research, Inc. v. Vitalink Comm. Corp., 55 F.3d 615, 619-20 (Fed. Cir. 1995). Claim terms "are given their ordinary and accustomed meaning unless examination of the specification, prosecution history, and other claims indicates that the inventor intended otherwise." Transmatic, Inc. v. Gulton Indus., Inc., 53 F.3d 1270, 1277 (Fed. Cir. 1995).

In order to arrive at the proper meaning of claims, the claims "must be read in view of the specification, of which they are a part." Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc) aff'd, 517 U.S. 370 (1996). Similarly, the claims must be read in light of the prosecution history. As the Federal Circuit has stated:

> If the claim language is clear on its face, then [the court's] consideration of the rest of the intrinsic evidence is restricted to determining if a deviation from the clear language of the claims is specified. A deviation may be necessary if "a patentee [has chosen] to be his own lexicographer and use terms in a manner other their ordinary meaning." Vitronics [Corp. v. Conceptronics, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)]. A deviation may also be necessary if a patentee has "relinquished [a] potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a reference." Elkay Mfg. Co. v. Ebco Mfg. Co., 192 F.3d 973, 979 (Fed. Cir. 1999). If however the claim language is not clear on its face, then [the court's] consideration of the rest of the intrinsic evidence is directed to resolving, if possible, the lack of clarity.

Interactive Gift Express, Inc. v. Compuserve Inc., 231 F.3d 859, 865 (Fed. Cir. 2000).

While "[e]xtrinsic evidence may always be consulted . . . to assist in understanding the underlying technology," it "may never be used 'for the purpose of varying or contradicting the terms in the claims.'" Id. at 866 (quoting Markman, 52 F.3d at 979). Reliance on extrinsic evidence is proper only where analysis of the intrinsic evidence leaves the claim unclear. Bell Comm., 55 F.3d at 619-20. Dictionaries, however, are a special form of extrinsic evidence, which courts may consider along with the intrinsic evidence as part of determining a claim term's ordinary meaning. Interactive Gift, 231

F.3d at 866.

2. Construction of Means-Plus-Function Elements Under 35 U.S.C. § 112, ¶ 6

Pursuant to 35 U.S.C. § 112, ¶ 6, a claim limitation may be recited in terms of a particular function to be performed, rather than the structure, material, or acts for performing that function. 35 U.S.C. § 112, ¶ 6. If the word "means" appears in a claim element in association with a function, § 112, ¶ 6 is presumed to apply. Micro Chem., Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1257 (Fed. Cir. 1999). Without the term "means," a claim element is presumed to fall outside § 112, ¶ 6, unless the element relies on functional terms rather than structure or material to describe performance of the claimed function. Id.

Where the patentees avail themselves of this means-plus-function claiming technique, the claim element "shall be construed to cover the corresponding structure . . . described in the specification and equivalents thereof." Id. The duty to link or associate structure to a claimed function is the quid pro quo for the convenience of employing the means-plus-function claiming technique of § 112, ¶ 6. B. Braun Medical Inc. v. Abbott Labs., 124 F.3d 1419, 1424 (Fed. Cir. 1997). Thus in construing a mean-plus-function element, the court must identify both the claimed function and the corresponding structure that is disclosed in the specification that is necessary to perform that function. See Micro Chem., 194 F.3d at 1258. However,"a court may not import functional limitations that are not recited in the claim, or structural limitations from the written description that are

unnecessary to perform the claimed function." Id.; see also Wenger Mfg., Inc. v. Coating Machinery Sys., Inc., 239 F.3d 1225, 1233 (Fed. Cir. 2001).

B. Construction of the '201 Patent

There are two claims of the '201 patent that are at issue in this suit. Both are independent claims. The first claim at issue is claim 1, and the second is claim 10. The court will construe each of these claims in turn.

1. Construction of Claim 1

Claim 1 is directed to a video signal processor. The video signal processor includes an input means, a statistical decoding means, a pixel interpolating means, an arithmetic data processing means, an output means, and a sequencing means.

Specifically, claim 1 of the '201 patent recites:

> 1. A video signal processor including:
>
> > input means for applying digital data representing a video image including compressed video data and pixel data, wherein a portion of said digital data is statistically encoded;
> >
> > statistical decoding means, coupled to said input means and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data;
> >
> > pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data;
> >
> > arithmetic data processing means, responsive to said control signal,

> for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means;
>
> output means, coupled to said arithmetic data output means, processing means for providing processed video data from said arithmetic data processing means as an output signal; and
>
> sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal.

Col. 60:4-35.

a. "Input means for applying digital data representing a video image including compressed video data and pixel data, wherein a portion of said digital data is statistically encoded."

The parties dispute the construction of the phrase "input means for applying digital data representing a video image including compressed video data and pixel data, wherein a portion of said digital data is statistically encoded." Both parties agree that this element is written in means-plus-function format and is thus subject to the requirements of § 112, ¶ 6. The parties also seemingly agree that the claimed function of the "input means" element is the phrase that follows the word "for" in the element: "applying digital data representing a video image, including compressed video data and pixel data, wherein a portion of the digital data is statistically encoded." The court agrees with the parties that this is the function of the "input means" and therefore adopts it as the court's construction of the function.

There is some disagreement between the parties as to the proper meaning of the

terms that comprise the function. For the sake of clarity, the court will construe these terms. First, the term "compressed video data" means video data that has been reduced to facilitate transmission or storage. Microsoft Computer Dictionary 102, 468 (4th ed. 1999). The term "pixel data" means decoded pixel data from a previously decoded video image. See col. 26:36-40 ("the pixel interpolator develops interpolated pseudo-pixel values, from the pixel values of a previous image, as a step in developing pixel values for the current image"). The ordinary meaning of the term "digital data [that] is statistically encoded" is digital data that is variable-length-encoded. See, supra I.B.2. Variable-length-encoding techniques, such as Huffman Coding, are discussed and referenced in the specification of the '201 patent. Col. 2:58-3:5. Thus, in more plain language, the function of the "input means" is applying digital data representing a video image, including compressed video data and decoded pixel data from a previously decoded video image, where a portion of the digital data applied by the input means is variable-length-encoded.

The parties dispute regarding this element centers on the corresponding structure that is associated with the input means. Intel claims that the corresponding structure in the specification for the input means is a data bus called "D BUS," which is represented in Figure 2. A "bus" is a data transmission path that interconnects different devices. Figure 2 discloses that the D BUS applies digital data including compressed video data and pixel data, a portion of which is statistically encoded, from VRAM 216 to the video processing circuitry 210. See col. 4:50-53 (broad arrows represent buses for conveying

multiple-bit parallel digital signals); see also col. 5:3-9 (compressed video signal data, which includes statistically encoded data, is stored in VRAM).

Broadcom disagrees with Intel's assertion that the structure disclosed in the specification that corresponds to the input means is the D BUS. Rather, Broadcom argues that, the patent identifies the specific circuitry associated with the VRAM control unit, the statistical decoder, and the input FIFO's as the corresponding structure for performing the input means function. In support of this contention, Broadcom points to several sections of the specification, that Broadcom characterizes as mandating the 'applying function' is performed by the structure identified by Broadcom above. First, Broadcom notes that the specification states that "the data provided by the source 212 is *applied* to a video random access memory (VRAM) 216 under control of a VRAM control unit." Col. 5:7-11 (emphasis added). Broadcom also draws support from another section of the specification that states that "[c]ompressed video signals are accessed via the statistical decoder 230 and the input FIFO's 232 and 234 under control of the sequencing circuitry 226."

First, it should be noted that the VRAM control unit cannot be included as part of the input means structure because it is a control element and cannot itself "apply data." The VRAM control unit does not perform the function of applying digital data; rather, it applies instructions to the off-chip VRAM. Consequently, the court will not consider the VRAM control unit as part of the corresponding structure of the input means. See Kegel

Co. v. AMF Bowling, Inc., 127 F.3d 1420, 1428 (Fed. Cir. 1997) (holding that a "controller" that activated the shifting of wicks was not part of the "means for selectively and independently shifting each of said wicks). The court will therefore consider whether the corresponding structure of the input means is the D BUS or the statistical decoder and the input FIFO's.

The ordinary meaning of "input," although somewhat circular, is "the means by which or the point at which an input (as of energy, material, or data) is made." Merriam-Webster New Collegiate Dictionary 591 (1981). Therefore, the ordinary meaning of an input means in the context of this invention is the path or point by which data enters a component. This definition, however, provides support for both parties positions. Intel interprets this term to mean that the structure is the data path that provides data to other components (the input FIFOs and the statistical decoder). Broadcom, however, interprets this term to mean that the structure associated with the function of "applying" is those other components themselves.

In light of the claim language, the court finds Intel's proposed construction to be more persuasive. The next element to be construed, the statistical decoding means, references the input means. That element claims a "statistical decoding means, coupled to said input means." Looking ahead, the parties agree that the structure associated with the statistical decoding means is the statistical decoder 230, the only statistical decoder described in the specification. If the structure associated with the input means included

the statistical decoder, the structure associated with the next element would the statistical decoder coupled (i.e. electrically connected) to itself. This reading would be strained. Standing alone, the input FIFOs cannot perform the claimed function because they do not process "statistically encoded data"; rather, they only process "pixel data." Thus, the better reading of the structure of the input means is the data path (BUS D in Figure 2) that connects components. Adopting this corresponding structure, the structure associated with the following element would be the statistical decoder coupled to a specific data path. This reading makes more sense.

The parties dispute as to the proper construction of the structure seems to center on the use of the term "apply" to describe the function. The word "apply," read in context of the specification, seems to be analogous with the word provide. See Col. 5:8-9 ("data provided by the source 212 is applied to . . . VRAM 216"). The specification also indicates that this apply/provide function is done via data buses. See Col. 5:42-46 ("data values provided . . . are applied to [components] via a bidirectional BUS B. The BUS B is also used to provide address values to the VRAM control unit."). Data BUS D is capable of performing the function of providing "digital data representing a video data and pixel data, wherein a portion of said digital data is statistically encoded." Accordingly, the court finds that the corresponding structure that is disclosed for the input means is BUS D.

b. "Statistical decoding means, coupled to said input means, and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data."

The parties dispute the construction of the phrase "statistical decoding means, coupled to said input means and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data." Both parties agree that this element is written in means-plus-function format and is thus subject to the requirements of § 112, ¶ 6. The parties also agree in the general sense that the function of the statistical decoding means is the phrase that follows the word "for" in the element: "decoding the statistically encoded digital data provided by said input means to generate decoded digital data." Broadcom, however, claims that decoding statistically encoded digital data means "to translate variable length encoded video data into fixed-length, 16-bit video data." Intel opposes reading into the claims the functional limitation requiring the result to be "fixed-length, 16-bit video data." Intel asserts that "decoded digital data" simply means digital data that has been decoded by reversing statistical (i.e. variable-length) encoding, and argues that the functional limitations urged by Broadcom are not included in the stated function. The court agrees, and declines to adopt Broadcom's proffered modifications to the stated function of this element. See Micro Chem., 194 F.3d at 1258 ("The statute does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.")

Turning to the corresponding structure, both parties agree that the corresponding

structure for the statistical decoding means is the statistical decoding circuitry 1014, see Fig. 10A, which is contained inside the functional box labeled statistical decoder 230 in Figure 2. This much is clear from the specification, which states: "The system includes a statistical decoder which generates fixed-length data values from variable-length-encoded data provided by a source of compressed video information." Col. 3:33-35. Furthermore, the specification states that Figure 10A "is a block diagram of a statistical decoder suitable for use in the video signal processing circuitry shown in Fig. 2." Col. 4:18-20. Figure 10A includes a box labeled "Statistical Decoding Circuitry (1014)," which contains the structure where the claimed function is performed. See 33:16-21.

While agreeing that this "black box" is the structure identified in the patent specification, Broadcom asserts that this disclosure alone is insufficient to comply with the requirements of § 112, ¶ 6. Broadcom points to a section of the specification that notes that:

> The statistical decoding circuitry 1014 used in this embodiments of the invention may, for example, be of the type described in U.S. Pat. No. 4,396,906 entitled "Method and Apparatus for Digital Huffman Encoding," which is hereby incorporated by reference. Col. 33:22-26.

Broadcom therefore claims that the structure of the statistical decoding means cannot simply be the "black box" shown in Figure 10A, but instead must include all of the detailed structural components of the statistical decoding circuitry that is shown and described in the '906 patent. In response, Intel asserts that, because such circuitry was

well-known in the art and performs a common electronic function, the black box disclosure is sufficient.

This difference of opinion regarding the structural sufficiency of black boxes is a recurring argument in the parties briefs with respect to numerous means-plus-function elements. The court will address this issue in the following paragraphs.

The patent law recognizes that developments in technology are often accomplished by building on the accomplishments of predecessors. Because of this recognition, patent disclosures do not require each patent to start from scratch and teach what is well-known already; rather, the disclosure of a patent should describe what is novel. See In re Gay, 309 F.2d 769, 774 (CCPA 1962) ("Not every last detail is to be described, else patent specifications would turn into product specifications, which they were never intended to be."); Loom Co. v. Higgins, 105 U.S. (Otto) 580, 586 (1881) ("That which is common and well known is as if it were written out in the patent and delineated in the drawings."). Therefore, the Federal Circuit has stated that "[a] patent need not teach, and preferably omits, what is well known in the art." Spectra-Physics, Inc. v. Coherent, Inc., 827 F.2d 1524, 1534 (Fed. Cir. 1997).

The statutory language of § 112, ¶ 6, however, requires the inventor to disclose "structure . . . described in the specification and equivalents thereof." 35 U.S.C. § 112, ¶ 6. As a quid pro quo for the convenience of employing means-plus-function claim language, the inventor has a duty to clearly link or associate structure to the claimed

function. B. Braun Med., Inc., 124 F.3d at 1424. In addressing whether a disclosure of structure is sufficient under § 112, ¶ 6, the Federal Circuit has stated that a court should "ask[] first whether structure is described in the specification, and, if so, whether one skilled in the art would identify the structure from the description." Atmel Corp. v. Information Storage Devices, Inc., 198 F.3d 1374, 1382 (Fed. Cir. 1999). Thus, once some structure in the specification is identified, even if that structure is a black box, the proper inquiry then turns to whether the patent discloses sufficient structure with which one skilled in the art could use to perform the function. See S3, Inc. v. nVIDIA Corp., 259 F.3d 1364, 1370-71 (Fed. Cir. 2001) (holding black box labeled "SEL" was sufficient structure because it was "a well known electronic structure and performs a common electronic function"); Budde v. Harley-Davidson, Inc., 250 F.3d 1369, 1381-82 (Fed. Cir. 2001) (holding that box labeled "Vacuum Sensor" and passage which notes that vacuum sensors were well known in the art at the time the patent issued sufficiently disclosed structure); Ampex Corp. v. Mitsubishi Elec. Corp., 966 F. Supp. 262, 270 (D. Del. 1997) (finding that to persons of ordinary skill in the art, block diagrams represent a number of different ways of implementing a circuit). The proper inquiry in this case therefore turns on whether the structure that is defined in the patent by a black box was well-known in the field of video compression and decompression at the time of the application of the patent.

In this case, it is clear that variable length (statistical) encoders were well known in

the art. First, the Background section of the patent specification itself explains that "Variable length statistical encoders which perform this type of compression are known in the art." See Col. 2:67-3:3. The patent specification also refers to U.S. Pat. No. 4,125,861, which describes such an encoder. A statistical decoder simply reverses the process applied by the statistical encoder. Thus, if statistical encoders were well known at the time the '201 patent was filed, so were statistical decoders.

This conclusion is further confirmed by the declaration of Intel's expert, Dr. Brian Von Herzen. Dr. Von Herzen identifies a number of patents which disclose statistical decoders that predated the filing of the '201 patent. Von Herzen Decl. ¶18. He also states that one of ordinary skill in the art at the time of the '201 invention could have constructed a statistical decoder. Id.

Moreover, the specification states that "Figure 10A is a block diagram of a statistical decoder suitable for use" in the patented video signal processing circuitry. Col. 4:18-20. The '906 patent was not the only known way to perform statistical decoding; it was merely an example of a device that was well-known in the art. See Budde, 250 F.3d at 1381-82 (distinguishing Atmel Corp. and noting that black box structure for vacuum sensor was sufficient because the record reflected that vacuum sensors were well known in the art). The inventors of the '201 patent should not be penalized by improperly limiting the structure of the statistical decoding means to that one embodiment. Accordingly, the court finds that the statistical decoding circuitry 1014 is sufficient to

impart the necessary structure for the "statistical decoding means."

It should be noted that the claim language also requires that the statistical decoding means be coupled (i.e. electrically connected directly or indirectly) to the input means, and be responsive (i.e. respond or react) to a control signal. The term "control signal" is a well-understood term in the art that means an electronic signal used to control internal or external devices or processes. See Microsoft Computer Dictionary 112 (4th ed. 1999). Naturally, the control signal itself is not a means-plus-function element, and is therefore not itself part of the structure that performs the function of the "statistical decoding means." See O.I. Corp. v. Tekmar Co., 115 F.3d 1576, 1581 (Fed. Cir. 1997).

c. "Pixel interpolating means, responsive to said control data signal and to the said input means for developing interpolated pixel values in said video image which are interstitial to pixels in said video image that are represented by said pixel data."

The parties dispute the construction of the phrase "pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data." Both parties agree that this element is written in means-plus-function format and is thus subject to the requirements of § 112, ¶ 6.

The parties agree that the function of the pixel interpolating means is the phrase that follows the word "for" in the element: "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image

that are represented by said pixel data." Within that phrase, the term "pixel data" again refers to decoded pixel data from a previously decoded image. The phrase "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data" indicates that pixel values are created for a current image being decoded that are between pixels from a previously decoded image. See Fig. 9A.

As described in the specification, in the context of moving images, a segment or region of an image may have been encoded by storing the direction and magnitude of movement in the segment relative to a corresponding segment contained in the previous image in the video sequence. See Col. 22:53-56. These movement values, or motion vectors, may be expressed in terms of fractions of the distance between pixels. However, because a video signal that is sampled at regular intervals can only be shifted by integer multiples of the horizontal and vertical distance between adjacent pixels, the processor uses circuitry called a pixel-interpolator to generate "pseudo-pixel" values to account for the fractional movements. Because these interpolated "pseudo-pixel" values are approximated values in between the actual pixel values, they are referred to as "interstitial" (i.e. in between) actual pixels. See col. 22:64-23:2; Col. 25:36-41; Microsoft Computer Dictionary 245 (4th ed. 1999); Webster's Third New Int'l Dictionary 1183 (Unabridged ed. 1986). The use of fractions in this manner increases the accuracy of the final image presentation.

The parties again dispute what should be included in the corresponding structure for the function of the pixel interpolator as described above. Intel urges the court to find that the "black box" block diagram labeled "Pixel Interpolator 246" in Figure 2 is the corresponding structure that is disclosed, because pixel interpolators were well-known in the art. Broadcom argues in response that the court should find that the more specific structure for the pixel interpolator found in Figure 8A is the disclosed structure.

The specification states that "Fig. 8A is a block diagram of the pixel interpolator used in the embodiment of the invention shown in Fig. 2." Col. 4:10-12. It is clear, therefore, that Figure 8A is a more detailed description of the structure inside the "black box" Pixel Interpolator 246 in Figure 2. If the inventors intended to disclose a generic pixel interpolator that was well-known in the art, they could have stopped their definition of the pixel interpolator at the "black box" of Figure 2 and said so. They did not. Accordingly, the court finds that to identify the corresponding structure merely as the "black box," without at least examining the more detailed disclosure to determine if it discloses structure that is required to perform the claimed function, would be disingenuous.

Intel, however, argues in the alternative that even if the court accepts Broadcom's argument with respect to Figure 8A, that the court should not find that all of the structure of Figure 8A is the "corresponding structure" for the pixel interpolation function. Intel claims that according to Federal Circuit precedent, the court must look to Figure 8A and

then parse it to determine what pieces of the structure disclosed within are "necessary" to perform the recited function of "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data." See Micro Chem., 194 F.3d at 1258 ("the statute . . . [does not] permit incorporation of structure from the written description beyond that necessary to perform the claimed function").

The court agrees the components in Figure 8A that are not necessary to perform the recited function of the pixel interpolating means should not be not included in the corresponding structure of that element. If the court included unnecessary structure as "corresponding structure," this would impermissibly narrow the claimed function.

According to the declaration of Dr. Von Herzen, the only elements within Fig. 8A that are necessary to perform the function of "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data" are registers 804 and 806 and adder 856. Von Herzen Decl. ¶ 26-27. Dr. Von Herzen supports this conclusion by examining the specification of the '201 patent, which provides the general equation for performing pixel interpolation and discloses that the basic operation of pixel interpolation is weighted averaging. In its simplest form, the pixel values A and B of two adjacent pixels are averaged. The average is the sum of two pixels divided by two. According to Dr. Von Herzen, the minimum logic structure needed to interpolate pixels in this simple manner

would be two registers to load and store the two pixel values to be interpolated and an adder whose output is wired to the output bus so as to shift the output down by one bit. He concludes that registers 804 and 806 and adder 856 or 858 suffices to perform the function.

Broadcom has not provided any declarations that support the conclusion that each of the twenty-two elements of the complex pixel interpolator disclosed in Fig. 8A is "necessary" to perform the claimed function. The court could rely on and adopt the three element structure consisting of register 804 and 806 and either adder 856 or 858 proffered by Intel in Dr. Von Herzen's declaration as the corresponding disclosed structure that performs the simple function of developing "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data." However, it would be inappropriate for the court to rely on one litigant's expert testimony without conducting an independent analysis. Thus, before relying on such extrinsic findings, a court should first closely examine the intrinsic record.

After examining the specification, the court declines to adopt Dr. Von Herzen's recommended structure because that structure over-simplifies the structure of a general linear pixel interpolator. First, while the specification notes that the pixel interpolator can be used "for averaging pixel values in either the horizontal or vertical direction," the specification clearly states that the main function of the pixel interpolator is "spatially

interpolating pixel values for a video image." Col. 31:40-44. If the structure were construed to yield a simplified device that only performs the simple function of averaging, as urged by Dr. Von Herzen, that structure would be incapable of performing the function of a basic linear pixel interpolator. The specification discloses the equation that is used for basic pixel interpolation. See Col. 25:55. This function is R = SF * (A-B) + B, where A is one pixel value, B is the second pixel value, and SF is a scale factor having fractional values between 0 and 1. R is the result of the pixel interpolation. When algebraically manipulated, this equation reads: R = SF * A + (1-SF) * B. See Col. 25:68. A pixel interpolator simply uses arithmetic logic components to perform the above function on inputted pixel values. The specification itself notes that "the combination of the subtractor 824, multiplier 825, and adders 856 and 858 is a linear interpolator." Col. 26:1-3. The two input pixel values may be provided to this series of components via input registers. Different scale factors can be provided to or preprogrammed into the multiplier. The court therefore concludes that the corresponding structure associated with the claimed function of "developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data" is subtractor 824, multiplier 825, adders 856 and 858, and two input registers, and equivalents of that structure. Each of these components are and were well-known in the art.

It should be noted that the plain language of the claim also requires that the

structure associated with the pixel interpolating means respond or react to the input means and to the same control signal that, as per the previous element, is sent to the statistical decoding means. As stated above, the control signal itself is not a means-plus-function element. See O.I. Corp., 115 F.3d at 1581.

d. "Arithmetic data processing means, responsive to said control signal, for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means."

The parties dispute the construction of the phrase "arithmetic data processing means, responsive to said control signal, for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means." Both parties agree that this element is written in means-plus-function format and is thus subject to the requirements of § 112, ¶ 6.

The parties agree that the function of the arithmetic data processing means is the phrase that follows the preposition "for" in the element: "for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means." The term "arithmetic operations" means addition, subtraction, division, and/or multiplication.

The parties again dispute what should be included in the corresponding structure for the function of the arithmetic data processing means as described above. Intel claims

that the corresponding structure of the arithmetic data processing means is the arithmetic and logic circuitry (ALC) that is associated with the arithmetic logic unit in Figure 2, which is a "black box" labeled 414 in Figure 4A of the patent. Broadcom, however, asserts that the corresponding structure is found in Figure 4B, which reveals the detailed circuitry that makes up the ALC depicted in Figure 4A. Broadcom claims that the corresponding structure is every component that is depicted in Figure 4B, including an "unconventional [dual-mode] adder."

The purpose of allowing parties to claim in terms of means-plus-function is to allow flexibility in claiming, so long as the patentee discloses some corresponding structure. If the court were to adopt Broadcom's claim that all of the elements in Figure 4B must be included, the claimed function would be narrowed from performing arithmetic operations on the two types of data that it receives as input to performing dual-mode 8-bit and 16-bit arithmetic operations. Such a construction would impermissibly incorporate unnecessary structure into the claimed function. See Micro Chem., 194 F.3d at 1258.

The court declines to accept Broadcom's argument that the inventors "chose not to disclose [conventional] adders in their patent because they did not contemplate using [such] adders in their invention." While it is true that the patent discloses an unconventional dual-mode adder, there is nothing in the specification that states that the function of the arithmetic data processing means could not be performed with a

conventional adder. In fact, in one of its modes, the dual-mode adder functions as a conventional adder. As the specification states, "To switch between providing a conventional ADD and a dual-add-with-saturate operation, an unconventional adder is used by the ALC 414." The patent notes that conventional adders are included as elements within the unconventional adder that is disclosed in Figure 4B: "The adders 450 and 452 [in Figure 4B] used in this embodiment of the invention are conventional eight-bit two's complement adders." Col. 14-61-63.

The patent specification makes clear that conventional adders were well-known in the art when the '201 patent was filed. For example, the patent states: "Conventional 16-bit arithmetic and logic circuitry would include a 16-bit adder capable of summing 16-bit two's complement numbers and a carry-in signal to produce a 16-bit two's complement output value and a carry-out signal." Col. 14:44-48. The patent specification also states that "the ALC used in this embodiment of the invention is exemplary. One skilled in the art of digital logic design may design and build alternative circuitry capable of performing equivalent operations to those described above." Col. 17:15-19.

The conventional adders 450 and 452 disclosed in Figure 4B can each independently perform arithmetic operations on the digital data provided by the statistical decoding means and on interpolated pixel values provided by the pixel interpolating means. The specification and associated flow-charts confirm that arithmetic operations performed on the "digital data provided by said statistical decoding means" may use

conventional adders to add statistically decoded data to other values. See Col. 59:31-44. Arithmetic operations performed on the "interpolated pixel values" may also use conventional adders, independently operating to add interpolated pixel values to other values. See Col. 56:38-50; col. 58:16-29. The additional elements disclosed in Figure 4B relate either to (i) added functionality to perform an addition function called "saturation" on the results of addition (e.g., gates 462, 464, 466, 468, 470, 472, 474, and 476), see col. 14:20-39; or (ii) additional functionality that allows for dual-mode functionality (e.g., split logic 454 and 456), see id. Neither of these functions are part of the required function of the arithmetic data processing means as claimed in claim 1 of the '201 patent. Accordingly, the court finds that the corresponding structure for the arithmetic data processing means is adder 450 or adder 452 as illustrated in Figure 4B and their structural equivalents.

It should again be noted that the claim also requires that the structure associated with the arithmetic data processing means respond or react to the control signal.

e. "Output means, coupled to said arithmetic data output means, processing means for providing processed video data from said arithmetic data processing means as an output signal; and"

The parties dispute the construction of the phrase "output means, coupled to said arithmetic data output means, processing means for providing processed video data from said arithmetic data processing means as an output signal." Both parties agree that this element is written in means-plus-function format and is thus subject to the requirements

of § 112, ¶ 6. The parties also agree that the claimed function of the output is "providing processed video data from [the] arithmetic data output means as an output signal."

In what has become a recurring theme, the parties again dispute the corresponding structure that performs the output means' claimed function. Intel claims that the corresponding structure is either the A BUS or the B BUS, as shown in Figure 2 of the specification, or both and the structural equivalents of each. Broadcom argues that the only corresponding structures identified in the specification that perform the claimed function are the output FIFO 236 and the VRAM control unit 238, both of which are shown in Figure 2. Broadcom identifies Figure 12A for the specific structure of the output FIFO 236. Broadcom identifies Figures 13A and 13B registers 1338 and 1342, control circuitry 1310, multiplexes 1356, and VRAM signal generator as the specific structure of the VRAM control circuit 238. All of the parties' proposed corresponding structures are shown in Figure 2 to be part of the on-chip video processor circuitry 210.

In support of its proffered construction of the corresponding structure, Intel first notes that Figure 2 shows that the A BUS or the B BUS pass data off-chip and provide an output signal that includes the results of the arithmetic data processing means. Intel also argues that Figure 4A shows the same thing. In Figure 4A the output of ALC 414 is provided to an output register 416 and then to a demultiplexer 418, from which the outputs are the A BUS and B BUS. The associated text in the specification explains that "[t]he result obtained by performing any of the operations shown in Table 3 is stored in

the output register 416. This register may be coupled to one or both of the busses A BUS and B BUS by the demultiplexing circuitry 418. . . ." Col. 17:9-14. Intel argues that Figures 2 and 4A support is construction that the "processed video data" output by the arithmetic processing means is placed in the A BUS, B BUS, or both.

To determine which of the proposed constructions is correct, the court turns to the specification. The section of the specification that introduces each of the components referred to above states:

> Data is provided by the circuitry 210 to the VRAM 216 via the output FIFO circuitry 236. The data values provided by the statistical decoder 230 and the input FIFO's 232 and 234 are applied to data path circuitry 242, an arithmetic and logic unit (ALU) 244 and a data RAM 228 via a bidirectional data bus B BUS. The bus B BUS is also used to provide address values to the VRAM control unit 238. A second bidirectional bus, A BUS is included in circuitry 201 to provide an alternate means for passing data values among the data path circuitry 242, ALU 244, and data RAM 228, and to provide data to and accept data from a pixel interpolator 246. In addition to the coupling set forth above, the data bus A BUS is connected to a microcode RAM and sequencer 226 and may be coupled to a microprocessor 224.

Col. 5:37-55 (emphasis added). The specification later elaborates on the output FIFO 236 in more detail stating that: "[the output FIFO 236] accept data in one or two bytes at a time from the pixel processing elements of the video signal processor 210, formats this data into 32-bit blocks and transfers these blocks to the VRAM 216." Col. 39:25-29. In describing the overall function of the video signal processor, the specification goes on to describe that after the arithmetic logic unit and pixel interpolator "expand the compressed

video signals and generate pixel values that describe the encoded image[,] [t]he generated pixel values are written into VRAM 216 via output FIFO 236 as a matrix having, for example, 240 rows and 256 columns . . . This matrix is hereinafter referred to as a bit-map." Col. 5:65-6:4. This bit-map is then read from the VRAM by the display processor which reproduces the decoded image onto the television, computer monitor, or other display device. See col. 6:5.

It can be seen from the above language that the specification explicitly links the claimed function to the output FIFO. The specification does not, however, link the claimed function with either the A BUS or the B BUS. In fact, while the output FIFO provides arithmetically processed data as an output signal to the VRAM (via the D BUS), neither the A BUS or the B BUS provide this output signal to the VRAM in Figure 2. Therefore, the court finds that the output FIFO is the corresponding structure for the output means. With respect to the VRAM control unit, the court finds that the VRAM control unit is not implicated in the claimed function of "providing processed video data from said arithmetic data processing means as an output signal." In the exemplary embodiment described in the specification, a signal from the VRAM control unit generates signals that instruct the output FIFO when and where to apply its output data to the D BUS so that data is properly transferred to the VRAM. This data transfer occurs after the output FIFO "provides [the] processed video data . . . as an output signal." Moreover, the specification also notes that while in one operational mode of the

exemplary output FIFO, data values are written to the VRAM using a given address value, the output FIFO also has a mode in which data values are written using successively increasing address values. Therefore, the VRAM control unit does not perform the claimed function of the "output means" and cannot be included as "necessary" corresponding structure.

With respect to the output FIFO, Intel argues that if the court decides that it is structure, the court should not incorporate all of the elements of Figure 12A as corresponding structure. Rather, Intel again urges the court to only determine which structural components are "necessary" to perform the claimed function. See Micro Chem., 194 F.3d at 1258. Intel argues that the specific multi-mode output FIFO described in Figure 12A, like the unconventional adder of Figure 4B contains numerous components that are unnecessary to perform the output means' function. Intel asserts that because output FIFOs were well-known in the art at the time of the '201 invention, see Von Herzen Decl. ¶ 36, the proper corresponding structure is the general "black box" FIFO shown in Figure 2.

As the court has noted in other sections of this memorandum opinion, the law is clear that a "black box" may be used to describe structural elements that are well-known in the art and perform a common electronic function. S3 Inc., 259 F.3d at 1371. The most general structural representation of the "output means" output FIFO is a box in Figure 2 labeled output FIFO 236. FIFOs, as explained earlier, are memory buffers that

are used to transfer data between different system components. Traditionally, such devices include stacks of registers and control circuitry that direct the input and output of the data that is stored in the registers. See, e.g., U.S. Pat. No. 4,151,609 ("First In First Out Memory," issued April 24, 1979). While the parties agree that Figure 12A and the associated text in the specification, which is labeled "circuitry suitable for use as the output FIFO 236," does not disclose a basic output FIFO, but instead describes a more sophisticated output FIFO that is capable of operating in different modes, see col. 39:53-43:64, Intel claims that not all of the circuit elements in this sophisticated output FIFO are necessary to perform the claimed function of the output means. After reviewing Figure 12A, the court agrees that the additional functionality provided by many of the elements within goes beyond providing the claimed function of the output means. Therefore, the court finds that the corresponding structure of the output means is a basic output FIFO and its equivalents, as represented by the block labeled FIFO 236 in Figure 2.

f. "Sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal."

The parties dispute the meaning of the term "sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal." Like the previous five claim

elements, the parties agree that the sequencing means of claim 1 is written in means-plus-function format. The claimed function is the phrase that follows the preposition "for" in the claim element: "generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal." The parties disagree as to other aspects of this claim element. First the parties dispute the meaning of the term "condition" as recited in the claimed function. Second, the parties dispute what is included as corresponding structure associated with the claimed function.

Intel argues that "to condition" means to assist or enable. In support of this definition, Intel states that the patent uses "conditioned" to mean "assisted" or "enabled" throughout the written description. See, e.g., col. 16:12-13 ("the ALC adder is conditioned to operate in its dual-add-with-saturate mode" by the microcontrol word [i.e., the control signal] issued by the microcontrol RAM and sequencer); col. 16:16-17 (the ALC adder may be "conditioned to operate as a conventional 16-bit two's compliment adder); col. 18:34-35 ("[u]nder the control of a microcode instruction, the gate 520 could be conditioned to join the busses A BUS and B BUS . . . .").

Broadcom, however, argues that term "to condition" means to instruct or set as a requirement. In support of this construction, Broadcom provides several dictionary definitions of the term "condition," which state that the term means "to set as a condition

or requirement" or "to adapt, modify, or mold to respond in a particular way" or "to set terms" or "to put into proper or the desired condition." See Webster's New World College Dictionary 290 (1996); The Merriam-Webster Dictionary 110 (1998); Webster's Third New Int'l Dictionary 473 (1993). Broadcom argues that Intel's proposed meaning of "to condition" as to assist or enable is inconsistent with the claim language and the specification's disclosure about the sequencer, which both state that the control signal generated by the sequencing means controls the components of the chip and that such components are responsive to the control signal. See Col. 6:66-7:6. Broadcom additionally asserts that the use of the term "condition" throughout the written description confirms its proposed meaning of the term. See, e.g., col. 8:61-63 ("During the instruction cycle T_0, the register MR0 is conditioned by the value of the signal A DST to store the 16-bit value MCO provided by the bus A BUS."); col. 26:62-64 ("The eight MSB positions of this 16-bit control value condition the pixel interpolator 246 to operate in its in-phase mode").

The court cannot find any support for Intel's argument that the term "to condition" means to enable or to assist. The court finds that the examples given by Intel regarding the use of the term "conditioned" in the specification do not necessarily support their proposed definition of the term because they are not inconsistent with the term's ordinary meaning. According to Merriam-Webster's Collegiate Dictionary, "conditioned" means "brought or put into a specified state." Merriam-Webster's

Collegiate Dictionary, available at <http://www.m-w.com/cgi-bin/dictionary> (last visited Oct. 29, 2001). Nothing in the claims or specification indicates that the patentees meant the term condition to be defined as something other than this ordinary meaning.

In line with the dictionary excerpts provided by Broadcom, the court finds that the meaning of the term "to condition" in the '201 patent is to put into a specified state. The sequencer conditions the statistical decoding means, the arithmetic data processing means and the pixel interpolating means by use of a control signal. As stated above, the term "control signal" means an electronic signal used to control internal or external devices or processes. See Col. 6:54 (equating the microcode control word that is the embodiment of the claimed control signal with "instructions"). As stated earlier, each of the above components is required by the claim language to be responsive to (i.e. each component must be able to respond or react to) this control signal such that when the control signal is received, the component is put into a specified state.

The second dispute between the parties on this claim element again concerns the structure that corresponds with "generating said control signal to condition said [circuit elements] to operate simultaneously to produce decoded and decompressed pixel data as said output signal." Intel argues that the corresponding structure is either (1) the on-chip microcode RAM and sequencer 226 shown in Figure 2 or (2) the off-chip (i.e. not within the video signal processing circuitry 210, which is indicated by a dotted line in Figure 2) microprocessor 224 shown in Figure 2. Broadcom, however, argues that while the

microcode RAM and sequencer 226 corresponds to the function of the sequencing means, the corresponding structure must be all of the detailed circuitry of that component, as disclosed in Figure 3A, and not a black box labeled microcode RAM and sequencer. Broadcom also argues that microprocessor 224 cannot be an alternative structural embodiment of the sequencing means because it is off-chip.

The specification describes the microcode RAM and sequencer circuitry 226 as "the central control element in the video signal processing circuitry 210." It is clear from the specification that the microcode RAM and sequencer circuitry is the component that generates the control signal. Col. 6:44-54. Intel argues that there is no need to delve into the underlying circuitry of the black box microcode RAM and sequencer circuitry of Figure 2 because RAM-based sequencers were well known in the art at the time of the invention. See Von Herzen Decl. ¶ 38 (citing several patents which show sequencers as black boxes and stating that "[a] broad variety of finite state machines . . . sufficient to generate control words for this type of application . . . have been in common use since at least the 1970's in integrated circuits"). While this might be true, the court finds it a more thorough approach to examine the most detailed disclosures for the corresponding structure that is necessary to perform the stated function. Where circuit diagrams are provided that describe "black box" elements those diagrams should be examined.

Figure 3A is "a block diagram showing circuitry suitable for use as the microcode RAM and sequencing circuitry of the video signal processing circuitry shown in FIG. 2."

Col. 3:53-56. Broadcom asserts that all of components in Figure 3A are corresponding structure for the sequencing means. Intel, however, argues that the only elements of Figure 3A that are necessary to perform the recited function are the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals. Von Herzen Decl. ¶¶ 39-40. This structure alone may perform the claimed function of a branching sequencer that can generate the control signal. In this arrangement, Dr. Von Herzen explains, instructions could be read out of a preprogrammed microcode RAM 310 into the instruction register 316. They would then be transmitted as the control word on the clock cycle following an active LI signal from the control block. The sequence of control words that would be sent to the instruction register could be conditionally changed (i.e. conditional branching operation) by the multiplexor 320, which could provide an alternative next instruction address to the control block. As an example, one can note that when microprocessor 224 assumes control over the microcode RAM and sequencer, it works in the manner similar to that described above by providing different control words directly to the instruction register 316 based on the clock cycle. In this case, after examining the specification, the court agrees with Dr. Von Herzen's proposed corresponding structure.

The specification describes the corresponding structure as follows: the microcode RAM 310 stores sets of control words (the control signal in this embodiment) in memory. These control words are sent to the instruction register 316, which, in response to a signal

LI generated by the control block 308 loads the control words to each of the components of the video signal processing circuitry 210. The multiplexor 320 provides an alternative next instruction address. The individual components of the circuitry 210 respond to the control signal provided by this structure to perform the decoding operation in a coordinated fashion. See Col. 6:40 - 7:7. Given that the other elements in Figure 3A are not necessary to perform the recited function, the court declines to include those elements in the corresponding structure of the sequencing means. Thus, the court finds that one corresponding structure for the sequencing means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and that structure's equivalents.

The court also declines to negatively construe the corresponding structure of the sequencing means to exclude "state machines," devices that proceed through a predefined and fixed series of inputs and produce a predetermined set of outputs. It is undisputed that state machines were well-known in the art at the time of the filing of the '201 patent. In fact, the patent discloses the use of state machines for some of the functional elements inside the VRAM control unit. See Col. 50:10-15. Broadcom argues that the claimed sequencing means must be construed as excluding state machines distributed in each functional block (such as the statistical decoder, the pixel interpolator, and the ALU) that synchronize the operation of the functional blocks, because the patentees could have included them in the patent, but chose not to. It is clear from the intrinsic record and from

the inventor's deposition that the use of state machines was never disavowed or disparaged. The inventor, David Sprague, quoted by Broadcom in its brief never said that a state machine would not work, but only that "we wanted . . . the capability of the chip to be programmable or reprogrammable." Because neither the patent nor the prosecution history said that state machines were incapable of performing the recited function, it is improper for this court to exclude state machines from the structure of the sequencing means during claim construction. See Micro Chem. Corp., 194 F.3d at 1255, 1260-61.

Intel also argues that the court should consider the off-chip microprocessor 224 as an alternative structure that performs the recited function. See Serrano v. Telular Corp., 111 F.3d 1578, 1583 (Fed. Cir. 1997) ("Disclosed structure includes that which is described in a patent specification, including any alternative structures identified"). The specification describes that by "[u]sing the signal HALT, the microprocessor 224 may effectively assume the control functions of the video signal processor 210." Col. 10:49-52; see also col. 10:53-67 (describing how microprocessor 224 controls the operation of the microcode RAM and sequencer circuitry). Both parties agree that microprocessor 224 is not implemented as part of the single integrated circuit 210; that is the microprocessor 224 is "off-chip."

Broadcom argues that, because the "video signal processor" recited in the preamble of claim 1 is the single chip integrated circuit that is labeled in Figure 2 as "video signal processing circuitry 201," the sequencing means must be part of the on-chip

video signal processing circuitry. Because microprocessor 224 is off-chip and not part of the video signal processing circuitry 201, Broadcom submits that it may not be an alternative structure for the sequencing means. Broadcom also argues that microprocessor 224, under control of the HALT signal cannot be an alternative sequencing means structure because it does not perform the recited function of the sequencing means, but instead inhibits the clock signal that is ordinarily used for directing the timing and sequencing of issuing control signals out of the instruction register 316 of the microcode RAM and sequencer. See Col. 10:43-48 (HALT signal "effectively freez[es] the internal state of the entire video signal processor 210").

While the preamble of claim 10 states that the elements of that claim are contained on a single "integrated circuit," the preamble of claim 1 is not so limited. It states that claim 1 relates to a "video signal processor" that includes the elements discussed above. Nothing in claim 1 requires the elements to be contained on a single chip. Therefore, if microprocessor 224 could independently perform the stated function of the sequencing means, the court would find it to be an alternative structure. There are two reasons why the court declines to include microprocessor 224 as an alternative structure. First, it does not perform the stated function of "generating said control signal to condition said [circuit elements] to operate simultaneously . . . ." Rather, its function, as described in the specification is "to cause the microcode RAM and sequencer circuitry 226 to write data into any register connected to the buses A BUS or B BUS or to load a bootstrap program

as set forth above." Col. 10:64-68. This functionality seems to describe a debugging feature, which allows a user to load instructions to the microcode RAM and sequencer circuitry one instruction at a time. This is not the stated function of the sequencing means. Second, the microprocessor is not a stand-alone component that can replace the circuitry of the microcode RAM and sequencer as an alternative structure than can perform the function instead; rather, the microprocessor can work with the microcode RAM and sequencer circuitry.

2. Construction of Claim 10

Claim 10 is directed to an integrated circuit for processing compressed video signals to provide decompressed video signals. The claimed integrated circuit includes an I/O port, an address output port, a statistical decoder, I/O circuitry, a pixel interpolator, an arithmetic processing means, a "selectively interconnecting" means, a control means, and an address generating means.

Specifically, claim 10 of the '201 patent recites:

> 10. An integrated circuit for processing compressed video signal, segments of which having been encoded using different encoding processes, to provide decompressed video signal representing moving images, said integrated circuit comprising:
>
> an I/O port for coupling said integrated circuit to memory means;
>
> an address output port for coupling address signals to said memory means;
>
> a statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals;

I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port;

a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal;

arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values;

means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means;

control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port; and

address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means.

Col. 61:45-62:33.

a. Preamble: "An integrated circuit for processing compressed video signal, segments of which having been encoded using different encoding processes, to provide decompressed video signal representing moving images, said integrated circuit comprising:"

Both parties agree that the preamble term "integrated circuit" means that the elements of claim 10 must be contained on a single chip. The court agrees. The ordinary meaning of "integrated circuit" is a device having a number of connected circuit elements fabricated on a single chip of semiconductor material. See Microsoft Computer Dictionary 238 (4th ed. 1999). This meaning is confirmed by the patent specification. See

Col. 4:62-63 (video processing circuitry 210 is implemented as a single integrated circuit); Fig. 2 (dotted line around circuitry 210). Thus, claim 10 recites a single chip for processing a compressed video signal.

b. "An I/O port for coupling said integrated circuit to memory means"

The parties dispute the term "an I/O port for coupling said integrated circuit to memory means." The parties generally agree that an "I/O port" is an interface on the integrated circuit through which input and output data may be transferred to and from the memory means. The court agrees and adopts this construction of I/O port.

The meaning of the terms "for coupling" and "memory means" is disputed. Broadcom asserts that the "for coupling" language requires that the I/O port couples, or electronically connects, the video processor integrated circuit to memory means that is external to the video processor chip. Broadcom then argues that because the dual-ported video random access memory (labeled VRAM 216 in Figure 2) is the only component external to the video processor chip disclosed in the patent that stores video data for the video processor chip, the meaning of the claim term "memory means" must be limited to a dual-ported video random access memory. In support of this argument, Broadcom cites the Federal Circuit case, Wang Labs, Inc. v. America Online, Inc., 197 F.3d 1377, 1383 (Fed. Cir. 1999) for the proposition that if the only embodiment described in the specification is a particular protocol, then the claims are properly limited to that protocol. Wang Labs, Inc., 197 F.3d at 1383 (holding that term "frame" is limited to character-

based frames and does not include bit-mapped frames).

The claim term "memory means" cannot be limited to the specific dual-mode VRAM that was used to describe the preferred embodiment, because the patentees did not claim "a dual mode VRAM." The patentee claimed a generic "memory means." It is undisputed that the term "memory means" is, and was at the time of the filing of the '201 patent, a term of art that is broadly defined as "memory or device where information can be stored and retrieved." Microsoft Computer Dictionary 285 (4th ed. 1999). Nothing in the specification compels a contrary or more limited construction. See Specialty Composites v. Cabot Corp., 845 F.2d 981, 987 (Fed. Cir. 1988) ("Where a specification does not require a limitation, that limitation should not be read from the specification into the claims").

In the Wang case cited by Broadcom, the issue for claim construction was whether the claim term "frames of information" covered both character-based and bit-mapped based protocols. The preferred embodiment was directed to character-based protocol systems, although the specification acknowledged that bit-mapped protocols were part of the prior art. The Federal Circuit found that the term "frame" as used in the context of the patent necessarily was limited to character-based protocols stating that "the specification would not be so understood by a person skilled in the field of the invention" to include protocols that were not specifically included in the specification. The Federal Circuit also noted the significant impact of the prosecution history on its finding. The prosecution

history of the patent at issue in Wang demonstrated that the patentee specifically distinguished the scope of the patent from prior art references relating to bit-map protocols. This confirmed the courts reading that claim's scope included only character-based protocols and not bit-map protocols.

The court reads the Wang case as standing for the proposition that patent claims should not be construed to cover embodiments that are not supported by the specification and are contradicted by the prosecution history. Wang is distinguishable from the instant case. In this case there is no such limiting prosecution history, nor does the specification compel the conclusion that the patented claims required a specific type of memory means.

Therefore, the court finds that the term "memory means" is to be accorded its ordinary meaning and defined as memory or device where information can be stored and retrieved. It is clear, however, from the claim language indicating that the I/O port is "for coupling said integrated circuit to memory means" that this "memory means" must not be contained as part of the single integrated chip, but is located off-chip. See also col. 45:3-6, 49-61 (referring to port as a location of a component for receiving data from, or sending data to, another component). If the memory means were on-chip, there would be no need to be able to couple it by using an I/O port.

With respect to the functional phrase "for coupling," the court finds that this phrase indicates only that the I/O port must be capable of being connected to an off-chip memory means and not that it is actually connected to such memory means. See, e.g.,

EcoLab, Inc. v. Envirochem, Inc., 264 F.3d 1358, 1366 (Fed. Cir. 2001) (functional language "for ware and hard surface washing" of the non-means-plus-function element "a three-dimensional, solid, cast, substantially uniform alkaline detergent for ware and hard surface washing required only that the recited detergent "be capable of 'ware and hard surface washing'").

c. "An address output port for coupling address signals to said memory means;"

The parties dispute the phrase "an address output port for coupling address signals to said memory means." The parties generally agree that the "address output port" recited in this element is an interface on the integrated circuit through which an address signal is output. See Microsoft Computer Dictionary 325, 349 (4th ed. 1999). This definition is also supported by the specification. See col. 50:62-65; Figure 13A (multiplexor 1356 of VRAM control unit issues address signals to the address/control bus labeled "AD/CT"). The court agrees and adopts this construction of address output port. More specifically, an "address signal" is a signal that specifies a location in memory in which data can be stored or from which data can be retrieved. See Microsoft Computer Dictionary at 17.

The parties again dispute the terms "for coupling" and "memory means." The court adopts its construction of those terms from its findings the preceding section. This construction is summarized in the following sentences. The term "memory means" means memory or device where information can be stored and retrieved. As per the claim language, the "memory means" must be contained off-chip. If it were not off-chip, there

would be no need to couple it to the chip. With respect to the functional phrase "for coupling," the court finds that this phrase indicates only that the address output port must be capable of being connected to an off-chip memory means and not that it is actually connected to such memory means.

d. "A statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals;

With respect to the next 3 elements of claim 10, the parties dispute whether they are written in means-plus-function format such that they invoke the requirements of § 112, ¶ 6. Specifically the parties dispute the meaning of the following three claim elements:

- "a statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals"
- "I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port"
- "a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal"

Because the parties argue whether each of these claims are claimed in mean-plus-function format, the court will address that threshold issue before turning to the construction of the claim language for each of the three elements.

Broadcom argues that the elements"statistical decoder," "I/O circuitry," and "pixel interpolator" are means-plus-function elements, which must be construed according to §

112, ¶ 6. Despite acknowledging that these elements do not contain the word "means," Broadcom nevertheless argues that these claim elements must be construed as means-plus-function elements because each of the elements simply recites a function but fails to recite any definite structure. See MAS Hamilton Group v. LaGard, Inc., 156 F.3d 1206, 1213 (Fed. Cir. 1998) (the phrase "lever moving element for moving the lever" is a means-plus-function element governed by 112, ¶ 6); C.R. Bard v. United States Surgical Corp., 102 F. Supp. 2d. 199, 215-16 (D. Del. 2000) (the phrase "surface of said hollow plug . . . being extremely pliable, allowing localized portions of the hollow plug to adapt to irregularities" is a means-plus-function element governed by 112, ¶ 6). According to the cases cited by Broadcom, when it is apparent that an element invokes purely functional terms without the additional recital of a specific structure for performing the function, the claim element may be a means-plus-function element despite the lack of express means-plus-function language. Broadcom argues that this is the case with respect to the three elements at issue here.

Intel argues that these elements are not means-plus-function elements. Intel first points out that when the term "means" is not used in a claim element, a presumption arises that 112, ¶ 6 does not apply. See Personalized Media Comm. LLC v. Int'l Trade Comm'n, 161 F.3d 696, 703-04 (Fed. Cir. 1998); see also Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 1318 (Fed. Cir. 1999) ("[W]hen an element of a claim does not use the term 'means,' treatment as a means-plus-function claim element is generally not

appropriate."); Greenberg v. Ethicon Endo-Surgery, Inc., 91 F.3d 1580, 1584 (Fed. Cir. 1996) ("[T]he use of the term 'means' has come to be so closely associated with 'means-plus-function' claiming that it is fair to say that the use of the term 'means' . . . generally invokes 112(6) and that the use of a different formulation generally does not").

Intel next argues that the functional language used in the claims does not equate to means-plus-function. See Greenberg, 91 F.3d at 1583 ("The fact that a particular mechanism . . . is defined in functional terms is not sufficient to convert a claim element containing that term into a 'means for performing a specified function' within the meaning of 112(6)"). Rather, because each of the three terms at issue "has a reasonably well understood meaning in the art" as the name for a structure, 112, ¶ 6 should not apply. Id.; see also Personalized Media, 161 F.3d at 705 (holding that "detector" is a sufficiently definite structural term to preclude the application of 112, ¶ 6, even though the detector was defined in terms of its function, because the term "detector" refers to a well-known structure for those knowledgeable in the art). Last, Intel contends that when a claim recites "means" language for some elements, but not others, the drafters presumably knew the difference and deliberately drafted the claim to reflect their intention that some elements should be construed as means-plus-function but that others should not be construed as means-plus-function.

As stated above, there is a rebuttable presumption in patent law that when a claim drafter fails to use "means" in a claim element that the claim element is not a means-plus-

function element. See Personalized Media, 161 F.3d at 703-04; Greenberg, 91 F.3d at 1580. That presumption may be overcome if the claim element only provides functional terms without the recitation of structure for performing that function.

In determining whether the claim language recites a structural term or merely recites functional terms, the court should read the claim language in light of both the specification and prosecution history. See C.R. Bard, 102 F. Supp. 2d at 216 (stating that review of prosecution history demonstrates that the examiner would not have allowed the claim but for examiners finding that claim limitation at issue was a "means" element). Moreover, a court should examine whether the claim element at issue has a well-understood structural meaning in the art. See MAS Hamilton Group, 156 F.3d at 1213 (holding that district court correctly held that "movable link member for holding the lever . . . " was a means-plus-function element because there was no evidence that a "movable link member" had a well-understood structural meaning in the art). In this case, the court finds no reason to overcome the presumption that the three elements at issue are not means-plus-function elements. First, it is undisputed that the terms "statistical decoder," "I/O circuitry," and "pixel interpolator" had reasonably well-known structural meanings to persons skilled in the art at the time of the '201 invention was filed. Von Herzen Decl. ¶¶ 11-27. Second, there is nothing in the specification or prosecution history that precludes these three terms from being defined by referring to their well-known general structures. Therefore, the claim elements convey sufficient structure such that they are

not defined purely in terms of their stated function.

Additionally, it should be noted that the claim drafters here used both means-plus-function language and non-means-plus-function language in the claims. Claim 1 recites "statistical decoding means," while claim 10 recites "statistical decoder." Claim 1 recites "input means" and "output means," while claim 10 recites "I/O circuitry." Claim 1 recites "pixel interpolating means," while claim 10 recites "pixel interpolator." In such instances, where there are no reasons for construing the latter terms as means-plus-function elements, a court should give effect to the intentional language used by the claim drafter.

The court finds that the "statistical decoder," "I/O circuitry," and "pixel interpolator" of claim 10 are not means-plus-function elements. Therefore, the court has no need to construe the function or the corresponding structure disclosed in the specification. The task for the court is merely to define those terms using ordinary claim construction rules.

The next claim term at issue is "a statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals." The term "statistical decoder" means a device that takes as input variable-length-encoded data and reverses the encoding process to provide decoded data as output. As stated previously, the term "coupled" means electronically connected, either directly or indirectly. The "said I/O port" refers to the "I/O port" that has been construed above in section II.B.2.b.

e. "I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port;

The parties dispute the meaning of the phrase "I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port." As stated in the preceding section, the court finds that this claim element is not a means-plus-function element. The term "I/O circuitry" means circuitry that inputs and outputs data. Examples of such circuitry are the input and output FIFOs in Figure 2. The remainder of the disputed terms have already been construed.

f. "A pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal;"

The parties dispute the meaning of the phrase "a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal." As stated above in section II.B.2.d., the court finds that this claim element is not a means-plus-function element. The term "pixel interpolator" means a device that calculates spatially interpolated pixel values, from the pixel values of a previous image, which approximate the values of fractionally offset pixels between pixels. See col. 22:64-23:13; col. 25:36-41. As noted above, the term "interstitial" is defined as relating to or situated within the space between things closely set. See Webster's Third New Int'l Dictionary 1183 (Unabridged ed. 1986); see also Fig. 9A (illustrating interstitial pixels).

g. "Arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values;"

The parties dispute the meaning of the phrase "arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values." Unlike the preceding three claim elements, the parties agree that this element is claimed in means-plus-function format. The court finds that the function of this claim element is "performing arithmetic and Boolean functions on binary values." "Arithmetic functions" are one or more of the operations of addition, subtraction, division, or multiplication. "Boolean functions" are one or more of the logical operations that can be performed on binary data such as AND, OR, NOT, or XOR. See Col. 13:Table 3. "Binary values" are data represented by 1s and 0s. Thus, the function of the "arithmetic processing means" is to perform operations which include both arithmetic functions (e.g., additional or subtraction) and boolean (e.g., AND or NOT) functions on data values represented by 1s and 0s.

The parties again dispute the corresponding structure for this claim element. Taking the same position with respect to this element as to the "arithmetic processing means" of claim 1, Intel argues that the corresponding structure of the claim 10 "arithmetic processing means" is the arithmetic and logic circuitry 414 depicted in Figure 4A. Broadcom, mirroring its position with respect to claim 1, argues that the corresponding structure of the "arithmetic processing means" is every element of the very detailed circuit diagram in Figure 4B. They claim that the corresponding structure must

be limited to the unconventional dual-mode adder described in that figure. As the court stated when addressing this argument in the context of claim 1 in section II.B.1.d., the elements that are not "necessary" to perform the claimed function, including the elements for performing the split-mode add-and-saturate function, will not be included in the corresponding structure.

In claim 1, the court found that performing "arithmetic operations" does not require the performance of both addition and subtraction. Rather, the court agreed with Intel that a structure that performs only successive addition operations, for example, satisfies the function of performing arithmetic operations. However, the court cannot simply apply its construction of the necessary corresponding structure of the arithmetic processing means of claim 1 to the arithmetic processing means of claim 10 because the two claim elements recite different functions. The function of the claim 1 arithmetic processing means is to perform arithmetic operations; however, the function of the claim 10 arithmetic processing means is to perform arithmetic operations and boolean functions. To satisfy the function of performing boolean functions a structure must be able to perform at least one of the boolean operations, such as the AND operation, for example. Therefore, the court finds that the corresponding structure of the claim 10 arithmetic processing means must include, in addition to the corresponding structure of the claim 1 arithmetic processing means, one or more of the Boolean logic gates (such as OR, NOR, XOR, AND, or NOT) depicted in Figure 4B. See Col. 13: Table 3 (displaying possible

combinations of arithmetic and logical functions that ALC 414 could be instructed to perform); Col. 13:31-43 ("The ALC 414 performs various arithmetic and logic operations on the values held in the register 410 and 412. . . the value held in bits 38-44 determine the function performed by the ALU according to Table 3 . . . . "). This construction is further supported by claim language in the "control means" element, construed infra in section II.B.2.i., which states that the control means conditions the arithmetic processing means "to perform one of a plurality of decoding algorithms." If the arithmetic processing means of claim 10 needs a control means to condition it to perform a "plurality" of functions it must have the capability of performing a set of functions. This can be satisfied by a structure that can perform at least one arithmetic function and at least one logical function.

As noted above, the claim language also requires the arithmetic processing means to be responsive to control signals that instruct the arithmetic processing means as to which function or sequence of functions it is to perform. See id. Broadcom seems to argue that this control signal is limited to the exemplary "48-bit microcode control word" used in the patent. The court finds that this is not the case. See Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 1054 (Fed. Cir. 1994) ("particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments").

h. "Means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means."

The parties dispute the meaning of the claim term "means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means." While agreeing that this claim element is written in means-plus-function format, the parties disagree as to the details of the stated function and the scope of the corresponding structure.

The function associated with the "means responsive to further control signals" is "selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means." Intel argues that the term "selectively interconnecting" refers to the ability to electronically connect and disconnect any of the recited elements (i.e., statistical decoder, I/O circuitry, pixel interpolator, and arithmetic processing means) to and from the other elements. Broadcom asserts that the term "selectively interconnecting" refers to the ability to electronically connect and disconnect any of the recited elements *to each other*. While this dispute might be semantic, the court will construe the function for the sake of clarity.

Intel, in its brief, states that the ordinary meaning of the term "interconnect" is "to connect mutually or with one another." Webster's Third New Int'l Dictionary 1177 (Unabridged ed. 1986). The court finds that applying this meaning to the claim element supports Broadcom's contention regarding the function of this element. The claim recites

that the function is to interconnect (i.e. to connect mutually) the statistical decoder, the I/O circuitry, the pixel interpolator, and the arithmetic processing means. Therefore, the applying Intel's proposed definition to the claim language itself reveals that the recited function is to connect the four stated elements to each other and not merely to connect those four elements to other elements on the chip. This meaning is supported by the specification as well. As shown in Figure 2, the four recited elements are not all connected to each other. For example, the only data bus to which the pixel interpolator is connected is the A BUS. The statistical decoder and I/O circuitry on the other hand, are not connected to the A BUS, but instead are connected to data buses B BUS and D BUS. Since the specification describes how each of these chip components works together to decode data, it makes sense that the function of the claimed means is to provide a structure that "selectively interconnects" these components to each other by coupling the A BUS and B BUS. E.g., Col. 18:18-24.

The parties also disagree as to the corresponding structure of this element. The parties agree that one corresponding structure is the register file 510 contained within the device labeled Data Path 242 in Figure2. Figure 5 shows a more detailed schematic of the Data Path circuitry from Figure 2 that includes the register file 510.

As shown in Figure 5 and explained in the specification, the register file 510, which includes four general purpose registers (R0, R1, R2, and R3), is connected to both the A BUS and the B BUS. See Col. 17:34-38. Thus the Data Path can receive data from

components that are connected to either of these busses. The specification explains that the Data Path "selectively interconnects" these components See Col. 17:32-18:38. In light of Figure 5, the court finds that the components in the Data Path that can perform this function are any one of the general purpose registers of the register file 510 or the bus gate 520. See Col. 18:30-38 ("it is contemplated that the bus gate 520 may, alternatively, be controlled by a bit in the microcode control word . . . [to] join the busses A BUS and B BUS . . ."). These components are, therefore, corresponding structures of the selectively interconnecting means.

Intel also argues that there are other components outside the circuitry within the data path that may be the corresponding structure. See Serrano, 111 F.3d at 1583 ("[d]isclosed structure includes that which is described in a patent specification, including any alternative structures identified"). In particular Intel argues that the following may also be corresponding structure: (1) input registers contained in the statistical decoder, pixel interpolator, and ALU; or (2) the register files DR0, DR1, DR2, DR3 contained in the data RAM 228, shown in Figure 6. Broadcom asserts that neither the input registers of the individual components or the register files of the data RAM are corresponding structure because the specification does not identify either of these potentially alternative structures as ones that perform, or are able to perform, the claimed function.

The court will first address the proposed alternative structure of the input registers of the individual components. According to the specification, the A BUS and B BUS are

both bidirectional busses. Each of the various components are coupled to these busses via their registers. See Fig. 10A (statistical decoder); Fig. 11A & col. 35:13-16 (input FIFOs); Fig. 12A, col 41:29-32 (output FIFOs); Fig. 4A & col. 13:25:3 (ALC). The specification further explains that in order to coordinate the bidirectional flow of data, each of the recited components of this claim element includes clock circuitry that enables and disables each element, thereby connecting and disconnecting each element from the data busses, and thus from the other elements. See Col. 12:1-26.

Upon reviewing the specification, the court finds that each recited component has an input register that is coupled to conventional circuits that interpret information contained in the control signal and thereby enable or disable the register. Id.; see, e.g., Fig., 10A (statistical decoder – register 1010 or 1016); Fig. 8A (pixel interpolator – register 802 or 812); Fig. 4A (ALU – register 410 or 412). Broadcom argues that these registers cannot perform the stated function because they simply store data. The court disagrees. The specification, as stated above describes an alternative mechanism for "selectively interconnecting" the recited components that uses the storage capabilities of the input registers and conventional decoding circuitry to perform this function. See Col. 12:1-26. The court therefore agrees with Intel that the input registers contained in the statistical decoder, pixel interpolator, and ALU comprise an alternative corresponding structure for the selectively interconnecting means.

Regarding the register files of the data RAM, the specification notes only that

these register files are used for "temporary storage of data values." Col. 18:41-42. The court, therefore, finds that these register files are not an alternative corresponding structure, because the specification never links that structure to the claimed function of selectively interconnecting.

i. "Control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port; and"

The parties dispute the meaning of the phrase "control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port." The parties agree that this element is claimed in means-plus-function format and that the function of the claimed "control means" is "generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port." As noted above, the term "control signal" means an electronic signal used to control internal or external devices or processes. The term "condition," as used in connection with the "control means" and as construed above means "to put into a specified state." Thus, to put it simply, the control signal contains instructions that are read by the arithmetic processing means. The arithmetic processing means responds to these instructions by performing the specified type of decoding called for in the control signal.

This function is described in detail by the specification. In the disclosed embodiment, areas of video image to be reconstructed by the video processor circuitry 201 are encoded, or compressed, into records called "cells" in terms of either absolute (intra-coding) or relative (inter-coding) bilinear polynomials (Ax + By + C), or as individually encoded pixels using a third encoding technique called "DPCM." Col. 51:62-52:9; see generally Col. 1:1-2:54. Under control of the sequencing circuitry 226, the compressed video data is applied to the arithmetic processing means and the pixel interpolator to expand the compressed video data and generate pixel values that describe the encoded image. Col. 5:61-67. As part of that process, the sequencing circuitry 226 sends control signals to the arithmetic processing means (ALU 414) to instruct that component to convert the compressed video data into bit-map pixel data by performing one of several decoding methods on the compressed video data that is provided at the data input/output port. Col. 6:66-7:6. The decoding operation can decode the absolute cells, relative cells, and DPCM cells. Col. 52:16-45.

Given this description, the parties agree that the corresponding structure to the control means is the microcode RAM and sequencer shown in Figure 2 as element 226. Col. 6:40-42 (microcode RAM and sequencer is central control element of video processing circuitry 201). The microcode RAM and sequencer 226 generates control signals and further control signals to selectively condition the arithmetic means to perform decoding algorithms on compressed video data. Col. 3:42-44; Col. 7:2-6.

However, Broadcom, as in its arguments about the sequencing means of claim 1, argues that the "black box" labeled microcode RAM and sequencer 226 is not sufficient structure, and instead urges the court to incorporate the detailed elements of that structure, as shown in Figure 3A. Intel, relying on its argument about the sequencing means of claim 1, responds that incorporating each and every element of Figure 3A would include structure that is not "necessary" to perform the claimed function. The court has addressed this issue in its discussion of the sequencing means of claim 1 and applies its construction of the corresponding structure of that element in section II.B.1.f. to the "control means" at issue in this section.

j. "Address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means."

The parties dispute aspects of the meaning of the phrase "address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means." The parties agree that this element is drafted in means-plus-function format and that the function of the "address generating means" is "generating memory address signals for said memory means." However, the parties dispute both the meaning of the term "memory means" and the proper corresponding structure that performs this function.

In section II.B.2.a. the court construed the term "memory means" to mean "memory or device where information can be stored and retrieved." This construction

applies to the term "said memory means" as used in this claim element.

The second dispute is what constitutes the corresponding structure for "generating memory address signal for said memory means." Intel identifies various on-chip registers (specifically:1) registers 1314 and 1318, 2) registers 1322 and 1326, 3) registers 1330 and 1334, or 4) registers 1338 and 1342, and structural equivalents of each of these register pairs) as the corresponding structure, while Broadcom argues that the only corresponding structure is the control circuitry 1310 and multiplexor 1356 of the VRAM control unit shown in Figure 13A and the structural equivalents of each. The key term in the recited function that the parties focus on in their dispute about the corresponding structure is the word "generating." Each party argues that the other's proffered construction is incapable of "generating."

Broadcom asserts that the on-chip registers do not generate address signals. Rather, Broadcom argues that these registers only *store* address values for the statistical decoder, input FIFOs, and output FIFO. According to Broadcom, the structure that actually generates the address signals sent to the VRAM is the control circuitry 1310 and multiplexor 1356 of Figure 13A. Broadcom argues that this circuitry together generates address signals that are outputted onto the AD/CTL (address/control) bus. The AD/CTL bus emanates from the multiplexor in Figure 13A and sends the address signals to the VRAM. Col. 50:62-65.

Intel, however, focuses on that section of the specification which notes that the

values held in registers 1314 and 1318, for example, are concatenated to form a 22-bit address value, which is "applied to an input port, O, of a multiplexor 1356." Col. 45:3-6. Intel asserts that because the multiplexor 1356 *receives* memory address signals, it is not the structure that generates them. Similarly, Intel argues that, according to the specification, the control circuitry 1310 does not itself generate memory address signals, but rather controls "the circuitry which stores the various address values" and "is primarily responsible for controlling the loading of address values for the various devices." Col. 44:37-46.

The verb "to generate" means to "bring into existence" or "to define (as a mathematical or linguistic set or structure) by the application of one or more rules of operations to a given quantity." Webster's Third New Int'l Dictionary 945 (unabridged 1986). In light of that definition and after reviewing the sections of the specification that each party set forth in support of its position, the court finds that the specification supports a finding that Broadcom's proposed structure is correct. The registers listed by Intel do not "generate" address signals. They store the address values of their respective components. While it is true that these stored address values are concatenated into a 22-bit address value, the registers' function is only to store the address values and not to intelligently compose the 22-bit address value.

One part of the structure that performs this function is the control circuitry 1310 (in Figure 13A) of the VRAM control unit displayed in Figure 2. The VRAM control

unit is provided with VRAM address values via the B BUS. Col. 5:45-47. The specification states that "[t]o store address values for [in this example] the input FIFO 232 multiplexors 1320 and 1324 are conditioned by a signal IFOM provided by the control circuitry 1310 to apply, respectively, the eight MSB's of an address value and the 14 LSB's of an address value to the input ports of registers 1322 and 1326, respectively." Col. 45:7-16. The specification goes on to describe that registers 1322 and 1326 load the values applied to their input ports in response to other signals generated by the control circuitry 1310.

The second part of the structure that performs the "address generating" function is the multiplexor 1356. The specification states that the concatenation of the 22-bit address values is completed when the values held in the registers are applied to the input ports of the multiplexor 1356. The address signal is then outputted to the VRAM, which is the "memory means" in this embodiment, by way of the AD/CTL bus. See Col. 50:62-65; Fig. 13A. Accordingly, the court finds that the corresponding structure of the address generating means is the control circuitry 1310 and the multiplexor 1356 and structural equivalents thereof.

III. CONCLUSION

The following table is intended to summarize, for the parties' convenience, the court's claim construction findings on the key disputed aspects of the claims.

Claim 1:	
input means for applying digital data representing a video image including compressed video data and pixel data, wherein a portion of said digital data is statistically encoded	The corresponding structure is the bus D BUS.
statistical decoding means, coupled to said input means and responsive to a control signal for decoding the statistically encoded digital data provided by said input means to generate decoded digital data	The term “control signal” means an electronic signal used to control internal or external devices or processes. The corresponding structure is the statistical decoding circuitry 1014, and structural equivalents.
pixel interpolating means, responsive to said control signal and to the pixel data provided by said input means for developing interpolated pixel values representing pixels in said video image which are interstitial to pixels in said video image that are represented by said pixel data	The corresponding structure is subtractor 824, multiplier 825, adders 856 and 858, and two input registers, and structural equivalents.
arithmetic data processing means, responsive to said control signal, for performing arithmetic operations on the digital data provided by said statistical decoding means and on the interpolated pixel values provided by said pixel interpolating means	The corresponding structure for the arithmetic data processing means is adder 450 or adder 452, and structural equivalents.
output means, coupled to said arithmetic data output means, processing means for providing processed video data from said arithmetic data processing means as an output signal	The corresponding structure for the output means is output FIFO 236, and structural equivalents.

sequencing means for generating said control signal to condition said statistical decoding means, said arithmetic data processing means and said pixel interpolating means to operate simultaneously to produce decoded and decompressed pixel data as said output signal.	The corresponding structure of the sequencing means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and structural equivalents. The term "to condition" means to put into a specified state.
Claim 10.	
an I/O port for coupling said integrated circuit to memory means	The term "I/O port" means an interface on the integrated circuit through which input and output data may be transferred to and from the memory means. The term "memory means" means memory or device where information can be stored and retrieved. The patent language indicates that the memory means must be contained off-chip. The term "for coupling" means capable of being connected.
an address output port for coupling address signals to said memory means	The term "address signal" means a signal that specifies a location in memory in which data can be stored or from which data can be retrieved.

a statistical decoder coupled to said I/O port for decoding variable-length-encoded compressed video signals	This claim element is not a means-plus-function element. The term “statistical decoder” means a device that takes as input variable-length-encoded data and reverses the encoding process to provide decoded data as output.
I/O circuitry coupled to said I/O port, for providing processed video signal to said I/O port, and for accepting a processed video signal from said I/O port	This claim element is not a means-plus-function element. The term “I/O circuitry” means circuitry that inputs and outputs data.
a pixel interpolator for generating values representing pixels interstitial to pixel values represented by said processed video signal	This claim element is not a means-plus-function element. The term “pixel interpolator” means a device that calculates spatially interpolated pixel values, from the pixel values of a previous image, which approximate the values of fractionally offset pixels between pixels. The term “interstitial” is defined as relating to or situated within the space between things closely set.
arithmetic processing means responsive to control signals, for performing arithmetic and Boolean functions on binary values	The corresponding structure of arithmetic processing means of claim 10 is the corresponding structure of the claim 1 arithmetic processing means and one or more of the Boolean logic gates (such as OR, NOR, XOR, AND, or NOT) depicted in Figure 4B, and structural equivalents.

means responsive to further control signals for selectively interconnecting said statistical decoder, said I/O circuitry, said pixel interpolator and said arithmetic processing means	The corresponding structure of the means responsive to further control signals is either 1) any one of the general purpose registers of the register file 510 ;2) the bus gate 520; or 3) the input registers contained in the statistical decoder, pixel interpolator, and ALU, and structural equivalents.
control means for generating said control signals and said further control signals to selectively condition said arithmetic processing means to perform one of a plurality of decoding algorithms on compressed video data provided at said I/O port	The corresponding structure of the control means is the microcode RAM 310, instruction register 316, multiplexor 320, and a portion of the control block 308 that generates the LI and MXC signals, and structural equivalents.
address generating means coupled to said address output port and responsive to at least said control means for generating memory address signals for said memory means	The corresponding structure of the address generating means is the control circuitry 1310 and the multiplexor 1356, and structural equivalents.