IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. ASUS COMPUTER INTERNATIONAL, INC., Defendant.	Civil Action No. 12-cv-210-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. TOSHIBA AMERICA INFORMATION SYSTEMS, INC., and TOSHIBA CORPORATION, Defendants.	Civil Action No. 12-cv-213-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. VIZIO, INC., Defendants.	Civil Action No. 12-cv-214-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. GOOGLE, INC. Defendant.	Civil Action No. 12-cv-1394-LPS

GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. HEWLETT-PACKARD COMPANY, Defendant.	:	Civil Action No. 12-cv-1395-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. LENOVO GROUP LTD., et al., Defendants.	:	Civil Action No. 12-cv-1397-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. ASUS COMPUTER INTERNATIONAL, INC., et al., Defendants.	:	Civil Action No. 13-cv-864-LPS

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MEMORANDUM OPINION

September 29, 2014
Wilmington, Delaware

STARK, U.S. District Judge:

Plaintiff Graphics Properties Holdings, Inc. ("GPH" or "Plaintiff") filed a patent infringement action against Defendants ASUS Computer International ("ACI"); Google, Inc. ("Google"); Hewlett-Packard Company ("HP"); Lenovo Holding Company, Inc. and Lenovo (United States) Inc. (collectively "Lenovo"); Toshiba America Information Systems, Inc. and Toshiba Corporation (collectively, "Toshiba"); and Vizio, Inc. ("Vizio") (collectively, "Defendants"). (C.A. Nos. 12-210, 12-213, 12-214, 12-1394, 12-1395, 12-1397, 13-864 D.I. 1) GPH asserts one or more of the following patents against each Defendant: U.S. Patent Nos. 6,816,145 ("'145 patent")[1], 6,650,327 ("'327 patent")[2], 8,144,158 ("'158 patent")[3], 5,717,881 ("'881 patent")[4], 6,359,389 ("'389 patent")[5], and 7,136,076 ("'076 patent")[6] (collectively, the

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[1] The '145 patent is entitled "Large area wide aspect ratio flat panel monitor having high resolution for high information content display." It was issued on November 9, 2004. (C.A. No. 12-210-LPS D.I. 1 Ex. B) (All citations to the record are to the docket in C.A. No. 12-210-LPS unless otherwise indicated.)

[2] The '327 patent is entitled "Display system having floating point rasterization and floating point framebuffering." It was issued on November 18, 2003. (C.A. No. 12-214-LPS D.I. 6 Ex. D)

[3] The '158 patent is entitled "Display system having floating point rasterization and floating point framebuffering." It was issued on March 27, 2012. (D.I. 8 Ex. C) The '327 and '158 patents share a common specification. The '158 patent is based on a continuation of the application that matured into the '327 patent.

[4] The '881 patent is entitled "Data processing system for processing one and two parcel instructions." It was issued on February 10, 1998. (C.A. No. 12-1394-LPS D.I. 1 Ex. A)

[5] The '389 patent is entitled "Flat panel display screen with programmable gamma functionality." It was issued on March 19, 2002. (C.A. No. 12-214-LPS D.I. 6 Ex. A)

[6] The '076 patent is entitled "System and method for providing a wide aspect ratio flat panel display monitor independent white-balance adjustment and gamma correction capabilities." It was issued on November 14, 2006. (C.A. No. 12-214-LPS D.I. 6 Ex. C)

"patents-in-suit"). Specifically, GPH currently asserts the '145 patent against ACI, Google, HP, Lenovo, and Vizio; the '327 and '158 patents against ACI, Google, Toshiba, Lenovo, and Vizio; the '881 patent against ACI, Google, and Lenovo; and the '389 and '076 patents against Vizio.

Pending before the Court is the issue of claim construction of various disputed terms of the patents-in-suit. The parties completed briefing on claim construction on March 7, 2014. (D.I. 182, 186, 198, 202) In addition to the briefing, the parties submitted technology tutorials (D.I. 195, 196) and expert reports (D.I. 183, 184, 187, 188, 199, 200, 201, 203, 204). The Court held a *Markman* hearing on April 24, 2014. (*See* D.I. 219)

I. LEGAL STANDARDS

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal quotation marks omitted). Construing the claims of a patent presents a question of law. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977-78 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370, 388-90 (1996). "[T]here is no magic formula or catechism for conducting claim construction." *Phillips*, 415 F.3d at 1324. Instead, the court is free to attach the appropriate weight to appropriate sources "in light of the statutes and policies that inform patent law." *Id.*

"[T]he words of a claim are generally given their ordinary and customary meaning . . . [which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13 (internal citations and quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Id.* at 1321

(internal quotation marks omitted). The patent specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

While "the claims themselves provide substantial guidance as to the meaning of particular claim terms," the context of the surrounding words of the claim also must be considered. *Phillips*, 415 F.3d at 1314. Furthermore, "[o]ther claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment . . . [b]ecause claim terms are normally used consistently throughout the patent . . . ." *Id.* (internal citation omitted).

It is likewise true that "[d]ifferences among claims can also be a useful guide . . . . For example, the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." *Id.* at 1314-15 (internal citation omitted). This "presumption is especially strong when the limitation in dispute is the only meaningful difference between an independent and dependent claim, and one party is urging that the limitation in the dependent claim should be read into the independent claim." *SunRace Roots Enter. Co., Ltd. v. SRAM Corp.*, 336 F.3d 1298, 1303 (Fed. Cir. 2003).

It is also possible that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316. It bears emphasis that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (internal quotation marks omitted), *aff'd*, 481

F.3d 1371 (Fed. Cir. 2007).

In addition to the specification, a court "should also consider the patent's prosecution history, if it is in evidence." *Markman*, 52 F.3d at 980. The prosecution history, which is "intrinsic evidence," "consists of the complete record of the proceedings before the PTO [Patent and Trademark Office] and includes the prior art cited during the examination of the patent." *Phillips*, 415 F.3d at 1317. "[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

A court also may rely on "extrinsic evidence," which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. For instance, technical dictionaries can assist the court in determining the meaning of a term to those of skill in the relevant art because such dictionaries "endeavor to collect the accepted meanings of terms used in various fields of science and technology." *Phillips*, 415 F.3d at 1318. In addition, expert testimony can be useful "to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of ordinary skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id.* Nonetheless, courts must not lose sight of the fact that "expert reports and testimony [are] generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence." *Id.* Overall, while extrinsic evidence "may be useful" to the court, it is "less reliable" than intrinsic evidence, and its consideration "is unlikely to result in a reliable interpretation of patent claim

scope unless considered in the context of the intrinsic evidence." *Id.* at 1318-19.

Finally, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007).

II. CONSTRUCTION OF UNDISPUTED TERMS

The parties have no dispute regarding the following terms. Accordingly, the Court will adopt these agreed-to constructions.

Patent-in-suit	**Claim Term**	**Agreed Construction**
'881	an instruction stream of two parcel items in sequence	Plain and ordinary meaning
'327/ '158	rasterization	A graphics operation that translates three dimensional primitives into a set of corresponding fragments and/or pixels and fills them in.
'327/ '158	a rasterization process	One or more of the rasterization processes (e.g., scan conversion, color, texture, fog, shading)
'327/ '158	coupled to	Associated in such a way that power or signal information may be transferred from one to another
'327/ '158	floating point format	A format for representing data by the sign and product of a fraction, or mantissa, and a number raised to an exponent
'327/ '158	s10e5	A 16 bit floating point format composed of one sign bit, ten mantissa bits, and five exponent bits
'327	fragment	A portion of a pixel

'145	light pipe	A structure that takes light from an external source or sources located along the edge or edges of a liquid crystal display and distributes the light across the viewing area of the display

III. CONSTRUCTION OF DISPUTED TERMS

A. The '881 Patent

1. "hardwired"

GPH the control functions for a digital computer system are generated by hardware using hardware logic design techniques [agreed construction in ITC Inv. No. 337-TA-884]
ACI A data processing apparatus that carries out operations directly in response to instructions without decomposing any operations into sub-operations.
Court the control functions for a digital computer system are generated by hardware using hardware logic design techniques

All defendants agree with GPH's proposal except for ACI. GPH's proposal is also the same construction that all parties involved in ITC Investigation No. 337-TA-884 agreed to. ACI argues that the patentee disclaimed claim scope when traversing U.S. Patent No. 4,099,229 to Kancler ("Kancler") and expressly limited claim scope such that a "hardwired" logic design technique must not decompose any operations into sub-operations. However, in addressing Kancler, the patentee actually provided a construction of "hardwired" that is consistent with GPH's proposal. (*See* D.I. 185 Ex. 11 at 6) During prosecution, the patentee stated that "[w]hen the control functions of a digital computer system are generated by hardware using hardware logic design techniques, the control unit is said to be 'hardwired.'" (*Id.*) Although the patentee distinguished "microprogramming" as an "alternative" to hardwiring, and went on to state that

"microprogramming can provide an elegant . . . method for generating the micro-operation sequences in a digital system," the patentee never stated that hardwiring could not perform similar micro-operations. (*Id.*) The patentee simply stated that it was more costly to use micro-programming to perform such operations "when the digital system is very simple and does not require any micro-operations or mini-control decisions." (*Id.*) Accordingly, the Court will not import ACI's proposed limitations into the "hardwired" term and will, instead, adopt GPH's broader construction.

2. "hardwired supercomputer"

GPH This term does not require construction. However, to the extent the Court disagrees that this term does need construction, it should be construed as: "hardwired high performance computer."
Defendants A hardwired computer that is among the fastest or most powerful of those available at a given time.
Google A hardwired computer designed to be exceptionally fast and powerful.
Court A hardwired computer designed to be exceptionally fast and powerful.

The term "hardwired supercomputer" appears only in the preamble of Claim 1. However, the Court finds that this term is limiting because it "recites essential structure" and is "necessary to give life, meaning, and vitality" to Claim 1. *See Catalina Mktg. Int'l. Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). "[C]lear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention." *Id.* at 808-09. During prosecution, the patentee used the term "hardwired

supercomputer" to distinguish Kancler and specifically limited Claim 1 to implementation using a "hardwired supercomputer." (*See* D.I. 185 Ex. 11 at 7-8)

The Court agrees with Google's construction of the term "hardwired supercomputer." (D.I. 176 Ex. A at 6-7) Plaintiff's construction is too broad and contrary to the prosecution history. In distinguishing Kancler, the patentee explained that the Kancler system "is not a 'supercomputer' processing system." (D.I. 185 Ex. 11 at 8) However, it appears Kancler is a "high performance computer" because Kancler teaches an "aerospace computer for missile flight control." (*Id.* Ex. 13 at 1:7-9, 2:44-54)

Defendants insist that their "construction would not mean that a supercomputer in 1989 would cease to be a supercomputer as technology progressed." (D.I. 42 C.A. No. 12-1394) However, Defendants' construction does not support this assertion. Google's construction more accurately captures the concept that a supercomputer is a computer that was designed such that it was exceptionally fast and powerful ***at the time it was designed***. Because the intrinsic evidence does not provide a construction for the "hardwired supercomputer" term, the Court looks to extrinsic evidence including the dictionary definitions provided by Defendants. (*See* D.I. 182 at 32) A hardwired supercomputer, therefore, is "a hardwired computer designed to be exceptionally fast and powerful."

3. "instruction fetch means for providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n"

GPH: Function: Providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n Structure: Program counter 126 coupled to instruction cache 110 over an address bus.

Defendants: Function: Providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n Structure: Instruction fetch port 112, instruction cache 110, and program counter 126.
Court: Function: Providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n Structure: Program counter 126 coupled to instruction cache 110 over an address bus.

The parties all agree that this term should be construed pursuant to 35 U.S.C. § 112, ¶ 6. The parties also agree on the definition of the function. The dispute is over the structure.

The structure identified by GPH is explicitly supported by the specification. The specification reads:

> Instruction data and tags are entered into the ***port 112*** from the arbitration node 44 as explained in the co-pending parent application. The instructions and tags are entered into the instruction cache 110 by way of holding elements 200 which form the input pipeline for the instruction cache. An ***instruction fetch means*** including ***a program counter 126*** transfers instructions in sequence to a pipeline including register holding elements 201 and 202 which form a pipeline between the ***instruction cache*** and the instruction decode and issue mechanism 122.

'881 Patent 9:31-41 (emphasis added). The specification distinguishes between the step of entering data in the "port 112" and describing the instruction fetch means. In disclosing the structure of the instruction fetch means, the specification only teaches the instruction fetch means as including "a program counter 126" and forming a pipeline between the "instruction cache and the instruction decode and issue mechanism 122." The specification does not teach data and tags entering the port 122 as part of the instruction fetch means.

Defendants argue that the patentee "unequivocally identified instruction fetch port 112 as necessary for performing the recited function." (D.I. 182 at 35) In summarizing the invention

during an appeal to the Board of Patent Appeals and Interferences, the patentee stated that:

> Instruction fetch means (see Figure 2, instruction fetch port block 112 and instruction cache block 110) provides an instruction stream of two parcel items in sequence. *See specification at page 42, lines 15-16.*

(D.I. 185 Ex. 18 at 3) However, as GPH correctly notes, in this portion of the prosecution history the patentee was merely summarizing the invention; it does not "specifically link" the instruction fetch means to the particular structure. The disclosure in the specification, by contrast, does link the instruction fetch means to the structure and is, therefore, the most relevant intrinsic evidence. Because GPH's construction most closely adheres to the specification, the Court will adopt it.

4. "instruction decode means responsive to each two parcel item for determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits"

GPH Function: Responsive to each two parcel item, determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits. Structure: Hardwired decode mechanism 122a an embodiment of which is further described by 3:4-8, 4:59-62, 9:41-44, 27:43-61, 33:1-5, 33:44-46, 35:16-20, Appendices A-B, and Figs. 2 and 7C.
Defendants Function: Responsive to each two parcel item, determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits. Structure: The specification does not disclose a corresponding structure, therefore, this limitation is indefinite under 35 U.S.C. § 112

Google Function: Responsive to each two parcel item, determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits. Structure: This limitation is indefinite under 35 U.S.C. § 112. The patent identifies the following blocks as performing instruction decode, though these blocks cannot perform the recited function: Fig. 2; the decode units (122a, 129a, 129b) of decode and issue mechanism 122, depicted in Figs. 7C-7D and described at 4:59-5:3, 27:53-61, 33:1-5.
Court Function: Responsive to each two parcel item, determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits. Structure: The specification does not disclose a corresponding structure, therefore, this limitation is **indefinite** under 35 U.S.C. § 112[7]

The parties all agree that this term should be construed pursuant to 35 U.S.C. § 112, ¶ 6. The parties also agree as to the function for this means-plus-function term. The parties disagree as to the corresponding structure for the recited function.

A structure disclosed in the specification qualifies as corresponding structure if the specification or the prosecution history "clearly links or associates that structure to the function recited in the claim." *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). In addition to disclosing corresponding structure, the patent's specification must provide "an adequate disclosure showing what is meant by that [claim] language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." *In re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed. Cir. 1994) (en banc). Therefore, "a means-plus-function clause is indefinite if a person of ordinary skill in the art would be unable to recognize

[7]Judge Gildea of the ITC also found the "instruction decode means . . . ." limitation to be indefinite. This Court has found Judge Gildea's analysis and holding persuasive.

the structure in the specification and associate it with the corresponding function in the claim." *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1311-12 (Fed. Cir. 2012); *see also generally Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014) ("[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.").

GPH contends that the associated structure is the hardwired decode mechanism disclosed in Figures 2 and 7C of the '881 patent. Defendants counter that (i) the disclosed figure, a box labeled "Instr Decode" (122a), does not disclose sufficient structure; (ii) the corresponding structure must include some form of circuitry showing how the function is performed by the alleged structure; and (iii) the structure must include decode units 129a and 129b, but is still indefinite.

According to Defendants, the inventive feature of the invention is its ability to determine, in one clock cycle, whether there are two parcel instructions or one. As such, according to Defendants, implementing this decoding is something that one of ordinary skill in the art could not have accomplished without additional structure defining how 122a operates. In distinguishing the invention from the prior art, the patentee stated that:

> Known prior art large hardwired processor systems require issuance of an n parcel instruction in n clock cycles. The cache delivers 64 bit instruction parcels. The present improvement decodes all 64 bits at once, examines the instruction fields, determines whether the 64 bits are one or two instructions, determines which instruction goes where and whether it goes on the first or second issue cycle. This decode mechanism is shown in FIGS. 7C-7D and includes decode units 122a, 129a, 129b.

'881 Patent 27:54-61. Although "determin[ing] whether the 64 bits are one or two instructions" may not be the sole inventive step of the '881 patent, it is an inventive step.

Plaintiff contends that "hardwired decode mechanism 122a" is sufficient structure to perform this function because the mechanism must (i) be hardwired, (ii) be digital logic, (iii) operate on op codes, (iv) get its input from the instruction register, and (v) output to the issue unit. (D.I. 219 at 173-82) Moreover, Plaintiff's expert Dr. Mangione-Smith, states that a "hardwired decoder circuit" is well known in the art and is the only structure recognized by the '881 patent that would be capable of carrying out the claimed function. (D.I. 188 at ¶¶ 40-41)

The Court disagrees with GPH that "hardwired decode mechanism 122a" is sufficient structure to perform the stated function. As the specification sets out, the instruction decode means (mechanism) includes decode units 122a, 129a, and 129b. *See* '881 Patent 27:54-61. One of ordinary skill in the art would not be able to discern the structure for the "instruction decode means" by reading the '881 patent specification. Although decoders may have been well known at the time of the invention, the '881 patent does not specifically state that "Instr Decode" box is a decoder. "A patentee cannot avoid providing specificity to structure simply because someone of ordinary skill in the art would be able to devise a means to perform the claimed function." *Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1385 (Fed. Cir. 2009). Although Plaintiff's expert, Dr. Mangione-Smith, was able to "derive" the structure from the "constraints of the '881 patent," the patent itself failed to specify the structure. *See Ergo Licensing, LLC v. Carefusion 303, Inc.*, 673 F.3d 1361, 1364 (Fed. Cir. 2012) ("[A] patentee is only entitled to 'corresponding structure . . . described in the specification and equivalents thereof, not any device capable of performing the function.'") The intrinsic evidence does not disclose the

hardware structure or the truth-tables needed to implement the instruction decode means in hardware. Accordingly, the Court agrees with Defendants that the "instruction decode means . . ." term is indefinite for failing to specify sufficient structure.

5. "one clock cycle"

GPH A measurement of a single unit of synchronizing time of a processor
Defendants A single period between successive rising edges or successive falling edges of the clock signal used to synchronize the instruction decode means and instruction issue means.
Court's Construction A single period between successive rising edges or successive falling edges of the clock signal used to synchronize the instruction decode means and instruction issue means.

Initially, the parties disputed whether the proposed constructions of "one clock cycle" sufficiently addressed the synchronizing role that the cycle played and whether the clock cycle could encompass more than one period between successive edges of a clock signal. Those concerns seem to have been addressed by the construction Defendants now propose. The Court will adopt Defendants' construction.

6. "said one clock cycle"

GPH *See* "one clock cycle"
Defendants The same single clock cycle in which the determining function is performed
Court's Construction *See* "one clock cycle"

The parties' dispute with respect to the clock cycle terms is centered on "said one clock cycle," not "one clock cycle." According to Defendants, "said one clock cycle" means the same

clock cycle as "one clock cycle." GPH contends that "said one clock cycle" means the same amount of time, i.e., the same period, as the "one clock cycle." According to GPH, if "one clock cycle" spans ten seconds between time t(0) and t(1), then "said one clock cycle" does not necessarily span the same ten seconds between t(0) and t(1). Instead, according to GPH, the "said one clock cycle" simply needs to be of the same length of time, i.e. ten seconds, as the "one clock cycle" recited earlier. The Court agrees with GPH.

In the specification, the patent teaches that "[i]n order to speed up processing of instructions in the improved processor of the present application, one or two parcel (32 or 64 bits) ***instructions*** are decoded and issued ***in one clock cycle.***" '881 Patent, 27:39-42 (emphasis added). According to Defendants, this recitation shows that the instruction needs to be decoded and issued in the ***same*** one clock cycle. But the specification does not read "in order to speed up processing of instructions in the improved processor of the present application, **[*a*]** one or two parcel (32 or 64 bit) ***instruction is*** decoded and issued in [***the same***] one clock cycle." Particularly because "instructions" is plural, the more natural reading of the specification is that the instructions are decoded and issued in different clock cycles of equal length.

Additionally, Fig. 7C of the '881 Patent shows the instruction decode step and instruction issue step occurring in two contiguous, separate pipeline time cycles. Adopting Defendants' proposed construction would seem to read this embodiment out of the patents.

Accordingly, the Court agrees with Plaintiff that "said one clock cycle" means the same time period as the clock cycle referenced earlier, but not the same band of time as the "clock cycle" in which the decoding occurs.

7. **"instruction issue means responsive to the instruction decode means for issuing each two parcel instruction for execution during said one clock cycle, and for issuing one then the other of the two one parcel instructions for execution in sequence during said one clock cycle and the next succeeding clock cycle"**

GPH Function: Responsive to the issue decode means, issuing each two parcel instruction for execution during said one clock cycle and issuing one then the other of the two one parcel instructions in sequence during said one cycle and the next succeeding clock cycle Structure: Hardwired instruction issue mechanism 122b and holding means 203 as further described by 3:4-12, 4:59-62, 9:41-10:1, 27:47-52, 33:1-5, 33:44-46, and Figs. 2 and 7C.
Defendants Function: Responsive to the issue decode means, issuing each two parcel instruction for execution during said one clock cycle and issuing one then the other of the two one parcel instructions in sequence during said one cycle and the next succeeding clock cycle Structure: The specification does not disclose a corresponding structure, therefore, this limitation is indefinite under 35 U.S.C. § 112.
Court Function: Responsive to the issue decode means, issuing each two parcel instruction for execution during said one clock cycle and issuing one then the other of the two one parcel instructions in sequence during said one cycle and the next succeeding clock cycle Structure: The specification does not disclose a corresponding structure, therefore, this limitation is **indefinite** under 35 U.S.C. § 112.[8]

The parties agree that this term should be construed pursuant to 35 U.S.C. § 112 ¶ 6. They also agree on the function. The dispute, again, is with respect to structure.

According to GPH, there is sufficient structure disclosed because the instruction issue means is a hardwired, digital circuit, the core logic of which is disclosed in the patent specification:

> The instruction cache delivers 64 bit entities (two 32-bit parcels) every clock cycle. Since the improved processor is adapted to

[8]Judge Gildea of the ITC also found the "instruction issue means . . . ." limitation to be indefinite. In coming to its own similar conclusion, the Court found Judge Gildea's analysis and holding persuasive.

> execute one and two parcel instructions, its decode mechanism determines which type of an instruction is being examined. If it is a two parcel instruction type and the instruction pipeline has not been stopped, the instruction is issued in one cycle. If the decode mechanism determines that the 64-bit entity comprises two 32-bit instructions, the two instructions are executed in respective clock cycles (two).

'881 Patent, 27:42-52. However, as Defendants point out, the patent specification, including the language quoted above, recites only functional language as it relates to the instruction issue means. GPH's proposed structure, "instruction issue mechanism 122b," does not disclose specific structure; it is instead a functional reiteration of "instruction issue means." *See, e.g.*, *Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1096 (Fed. Cir. 2008) ("[T]he unadorned term 'mechanism' is simply a nonce word or a verbal construct that is not recognized as the name of structure and is simply a substitute for the term 'means for.'"). The fact that it is "hardwired" similarly adds little in the way of structure necessary for performing the recited function. Although GPH's expert opined that the recited function could be performed using AND gates, the physical circuit that would implement the "hardwired instruction issue mechanism" is never disclosed in the specification. *See Blackboard, Inc.*, 574 F.3d at 1385 ("A patentee cannot avoid providing specificity to structure simply because someone of ordinary skill in the art would be able to devise a means to perform the claimed function."); *Ergo Licensing, LLC*, 673 F.3d at 1364 ("[A] patentee is only entitled to 'corresponding structure . . . described in the specification and equivalents thereof, not any device capable of performing the function.'").

As the "instruction issue means" is not supported by corresponding structure, it is indefinite.

B. The '327 Patent

1. "rasterization circuit"

GPH: An interconnection of specialized electrical hardware for performing rasterization, such as one or more of the processes of scan conversion, assigning colors, lighting, applying texture, applying fog, blending shading, and antialiasing
Defendants: One or more separate circuits each of which performs only one rasterization process (e.g., scan conversion, assigning colors, lighting, applying texture, applying fog, shading, and antialiasing)
Court: An interconnection of specialized electrical hardware for performing rasterization, such as one or more of the processes of scan conversion, assigning colors, lighting, applying texture, applying fog, blending shading, and antialiasing

Initially, the dispute between the parties was whether the rasterization circuit must be a separate circuit dedicated to a specific rasterization process or whether it merely needs to be specialized to perform any of the listed rasterization processes, including scan conversion, assigning colors, lighting, applying texture, applying fog, blending, shading, and antialiasing. Defendants contend that the "rasterization circuit" needs to be separate for each specific rasterization process because the claims explicitly list and couple the rasterization circuit with various rasterization processes. GPH does not disagree with this position:

> THE COURT: So he says that the patentee chose not to draft claims with the structure with the three A, B, C, his circuit on top of one another. A computer system comprising, one or more circuits for performing functions A, B, and C. Is that what you [are] intending to cover?
>
> MR. SCHECTER: No, we're not. We're not. And that is what I meant when I said we're not requiring. ***We would not say that three separate circuits that are identical to each other, that have identity could***

> ***in fact meet the limitations of the claims. You would need separate circuits.*** You need circuits that are distinct, that are coupled to, that actually can share signal information, power information with one another.

(D.I. 219 at 38) (emphasis added) Although Defendants' construction includes the phrase "performs only one rasterization process," Defendants actually contend:

> Now, you talk about, I think what happened in some of the other cases is plaintiff argued that "dedicated" means "exclusive," and something can't be exclusive. They didn't want to do that. Well, we're not saying that. By separate, for example, we're saying the B circuit here is separate from the A circuit. ***Could the A circuit that performs function A also perform a function B that is not recited in the claim? Perhaps. That doesn't matter.*** It's possible by the claim, but in order to infringe the claim, they just need to point to one thing: an A circuit that performs function A, something else that is coupled to it that is a B circuit that performs function B.

Id. at 24-25 (emphasis added). Thus, Defendants' construction does not capture their actual position.

Another problem with Defendants' construction is it lacks support in the intrinsic record. Defendants point to no specific claim disavowal or any support in the record for a construction that limits "rasterization circuit" to a dedicated circuit that performs only one rasterization process.

Plaintiff's construction is supported by the record. As GPH points out, the claims couple multiple circuits that carry out the rasterization process. Claim 2, for example, couples a texture memory with a texture circuit as part of the rasterization process. Similarly, Figure 4 of the '327

Patent depicts "[a] single block 410 [that] is used to accomplish texturing, fog, and anti-aliasing." '327 Patent at 11:15-17. Additionally, the specification discloses using specialized graphics hardware, including in Figure 1, which distinguishes a general "Processor" from a "Graphics Subsystem." These disclosures show specialized hardware for performing rasterization. The Court will adopt Plaintiff's construction.

2. "rasterization process which operates on a . . . floating point format"

GPH One or more of the rasterization processes (e.g., scan conversion, color, texture, fog, shading) operate on a floating point format
Defendants A "rasterization process" that operates entirely on floating point values in performing all calculations of that process.
Court One of more of the rasterization processes (e.g., scan conversion, color, texture, fog, shading) operate on a floating point format

According to Defendants, the rasterization process operations must occur entirely on floating point values when performing all calculations for a particular rasterization process. To support this position, Defendants cite to the "Summary of the Invention" in the specification. There, the specification states that in "[t]he present invention . . . certain rasterization processes are performed according to a floating point format. Specifically, the scan conversion process is now handled entirely on a floating point basis. Texturing, fog, and antialiasing all operate on floating point numbers. The texture map stores floating point numbers." '327 patent 4:7-24. Defendants contend that use of the "the present invention" language limits the scope of the invention. (D.I. 219 at 50-51; *see also Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) (stating that "describ[ing] the features of the 'present invention' as a

whole . . . limits the scope of the invention"). As with claim construction generally, however, the phrase "the present invention" must be read in context, with a fair appreciation of the entirety of (at least) the intrinsic evidence. While "[t]he public is entitled to take the patentee at his word," *Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006), it is equally true that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction," *Liebel-Flarsheim Co.*, 358 F.3d at 906. In the '327 patent, the written description makes clear that "[i]t should be noted that although many of these blocks are described above in terms of floating point, one or several of these blocks can be performed in fixed point without departing from the scope of the present invention." '327 patent 11:38-46. Thus, in the overall context of the specification, the single use of the phrase "present invention" in the '327 patent is not limiting.

In fact, even the portions of the specification to which Defendants cite actually support GPH's position that the rasterization processes need not operate exclusively on floating point and that, instead, some of the calculations may be performed in non-floating point format. For example, the specification states "it has been discovered by the present inventors that it is now practical to implement ***some portions or even the entire rasterization process*** by hardware in a floating point format." '327 Patent 2:54-57 (emphasis added). Thus, although using floating point is encouraged by the specifications, neither the claims nor the specification limit all calculations associated with rasterization exclusively to floating point. Accordingly, the Court will adopt GPH's proposed construction. *See Silicon Graphics, Inc. v. ATI Technologies, Inc., et al.*, 607 F.3d 784, 790-91 (Fed. Cir. 2010) (similarly construing same term).

3. "frame buffer"

GPH A portion of computer memory which must store color values and may do so during and/or after rasterization.
Defendants Final stage memory that stores at least the floating point color values, for pixels of one or more frames, that are ready for display and that could be scanned out for display or fed back for additional processing.
Court A portion of computer memory which must store color values and may do so during and/or after rasterization.

GPH contends that a frame buffer merely needs to store color values and do so during and/or after rasterization. Defendants agree that the frame buffer must at least store color values but do not agree that the color values are stored during rasterization. Defendants contend that the frame buffer must also (i) be the final stage memory, (ii) store color values in floating point format, and (iii) store pixels of entire frames. The Court does not find support in the intrinsic record for any of the additional limitations proposed by Defendants. Accordingly, the Court adopts GPH's proposed construction.

Defendants' first limitation, that the frame buffer be the "final stage memory," is undercut by Defendants' concession that the color values could be "scanned out for display or fed back for additional processing." Because the patent discloses a multipass architecture, *see, e.g.*, '327 Patent at 9:35-49, the Court does not find support for the "final stage memory limitation." In fact, the specification supports the opposite conclusion – that data may be stored in the frame buffer before rasterization is complete. *Id.* at 10:5-7 ("Therefore, in the present invention the data are read from the frame buffer, operated on, then written back into the frame buffer."). The specification also supports GPH's contention that the frame buffer may store color values

"during and/or after rasterization." *Id.*

Defendants' contention that the frame buffer must store color values in floating point format is also not supported by the intrinsic evidence. Again, the intrinsic record points to the opposite conclusion: that there is no requirement that the frame buffer store values in floating point format. The specification states:

> The resulting floating point values are stored in the frame buffer 522 . . . . Again, it should be noted that one or more of the above blocks can be implemented in a fixed point format without departing from the scope of the present invention. However, the blocks of particular importance for implementation in a floating point format include the polygon rasterization 501, texel generation 506, texture memory 507, fog 509, blending 516, and frame buffer 522.

Id. at 12:23-33 (emphasis added). Although the specification does explicitly note that it is of "particular importance" that the frame buffer be implemented in floating point format, the specification does not mandate such a limitation. More importantly, only certain – and not ***all*** – of the claims are limited to a floating point frame buffer. *See id.* at Claim 22 ("A computer system having a floating point frame buffer . . . .").

Finally, the Court finds no support in the intrinsic record for the limitation that a full frame must be stored in the frame buffer. Defendants argue that "[t]he frame buffer must be capable of storing a complete frame of image data because it is the final step in the graphics pipeline." (D.I. 182 at 22) As the Court does not find that storing data in the frame buffer is the last step before a graphic is displayed, the Court does not find Defendants' argument persuasive. Accordingly, the Court rejects the limitations proposed by Defendants and will, instead, adopt Plaintiff's construction.

4. "color values"

GPH Attributes of a color (e.g., proportion of red, green, and blue color components).
Defendants Floating point values representing a color assigned to a fragment or pixel to be displayed on a display screen.
Court Attributes of a color (e.g., proportion of red, green, and blue color components).

Defendants' construction of the "color values" term imposes three limitations that GPH's construction does not contain. Defendants require that the color values be floating point values, that those values be assigned to a fragment or pixel, and that those fragments or pixels need to be displayed on a display screen.

To support the position that "color values" must be in floating point format, Defendants cite to the Summary of the Invention, which states that "[a]ttributes associated with pixels and fragments are defined in a floating point format. In particular, all color values exist as floating point format." '327 patent col 4:12-16. However, in the claims, the patentee distinguished between "floating point color values" and "color value" without the "floating point" modifier. *See, e.g.*, *id.* at Claim 1 (first reciting "a frame buffer coupled to the rasterization circuit for storing a plurality of color values" and then separately claiming "wherein the rasterization circuit performs scan conversion on vertices having floating point color values"). The Court finds the differentiation in the claim language to be more compelling than the language in the Summary of the Invention. Thus, the Court will not limit the claims to "floating point" color values.

Next, Defendants contend that the color values must be assigned to fragments or pixels. However, as Judge Gildea noted in his construction of this term, Defendants'

> proposed construction adds limitations not expressed or implied in the asserted claims nor justified by the specification or intrinsic record as a whole. A 'color assigned to a fragment or pixel to be displayed on a display screen' leaves open to interpretation what, how, and when a color is 'assigned' and thereby renders the proposed construction ambiguous.

337-TA-884, [Corrected] Order No. 52 Construing the Terms of the Asserted Claims of the '158 and '327 Patents, March 5, 2014, p. 33. The Court agrees with Judge Gildea that Defendants' proposed limitation that the color values be "assigned to fragments or pixels" finds no support in the intrinsic record. As such, the Court will not read this limitation into the claim.

Finally, Defendants propose the "to be displayed on a display screen" limitation. However, as with "frame buffer" earlier, GPH points out that the color values may continue to undergo transformation or may be blended and never appear on a display screen. In particular, Figure 5C illustrates two outputs of the frame buffer. One goes to the display but the other goes to the blending block. Adopting Defendants' construction would read out the possibility that the frame buffer can output to the blending block.

Accordingly, the Court rejects all three limitations proposed by the Defendants and will adopt GPH's proposed construction.

5. "per-fragment operations"

GPH Graphics processing steps within rasterization including one or more of pixel ownership, scissor test, alpha test, stencil test, depth buffer test, dithering, and logic operations.
Defendants Two or more graphics processing steps including two or more of pixel ownership, scissor test, alpha test, stencil test, depth buffer test, dithering, and logic operations.
Court Graphics processing steps within rasterization including one or more of pixel ownership, scissor test, alpha test, stencil test, depth buffer test, dithering, and logic operations.

The parties' primary dispute with respect to the "per-fragment operations" term is whether the circuit must perform two or more per-fragment operations. GPH contends that this "two or more step" limitation is not supported by the intrinsic record. The Court agrees.

Defendants suggest that because the term "operations" is plural, the circuit must perform at least two operations. However, in context it is clear that "operations" is plural because any given operation must be performed several times, and several operations need to be performed on a per-fragment operation before the relevant values may be stored. *See* '327 patent col. 11:35-38 ("But before the floating point values are actually stored into the frame buffer 412, a series of operations are performed by per-fragment operations block 411 that may alter or even throw out fragments."). Plaintiff's construction is supported by the specification. *See id.* col. 12:1-23. Accordingly, the Court will adopt Plaintiff's construction.

6. "logic"

GPH Plain and ordinary meaning.
Defendants Separate, hardwired circuitry consisting of logic gates.
Court Hardwired circuitry consisting of logic gates.

Defendants contend that "logic" as used in the patent must be hardwired and must be "separate." As with Defendants' previous arguments related to "dedicated" or "separate" circuitry, the Court finds that this proposed limitation is not supported by the intrinsic record and does not clarify the disputed term. However, the requirement that logic be hardwired is supported by the specification. *See* '327 patent col. 2:51-57 ("[I]t has been discovered by the present inventors that it is now practical to implement some portions or even the entire

rasterization process by hardware in a floating point format."). Hence, the Court will adopt the "hardwired" limitation proposed by Defendants but not adopt the "separate" limitation.[9]

C. The '158 Patent

1. "geometry processor"

GPH A processor for performing geometric calculations on a plurality of vertices of a primitive.
Defendants A separate processor that performs geometric calculations on a plurality of vertices of a primitive.
Court A processor for performing geometric calculations on a plurality of vertices of a primitive.

The sole dispute with respect to the "geometry processor" term is whether the processor needs to be a "separate" processor. For the reasons discussed with respect to the "rasterization circuit" and "logic" terms above, the Court will reject Defendants' proposed limitation here as well.

Defendants support their construction by citing to the Background Art section of the '158 patent, which states that "[i]n order to increase the speed and increase graphics generation capability, some computer systems utilize a specialized geometry engine, which is dedicated to performing nothing but geometric calculations." '158 Patent at 2:23-26. However, as Plaintiff correctly points out, a discussion in the prior art section of a patent on what "some computer systems utilize" does not necessarily limit the claims of this patent. Without a clearer disavowal

[9]Throughout this Opinion, unless the Court indicates that "no construction is necessary" or that the "plain and ordinary meaning" applies, the Court has determined that the parties have raised an actual dispute regarding the proper scope of the claims, which the Court must resolve by claim construction. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008).

of claim scope, the Court will not read in the limitation that circuits may not share components to perform specialized functions. Accordingly, the Court will reject Defendants' "separate processor" limitation and adopt Plaintiff's construction instead.

2. "scan converter"

GPH A subsystem that receives primitives and generates pixel and/or fragment positions associated with the primitive.
Defendants A circuit that performs the process of specifying which pixels of the display screen belong to which primitives on an entirely floating point basis.
Court A subsystem that receives primitives and generates pixel and/or fragment positions associated with the primitive.

There are two primary disputes with respect to the "scan converter" term. First, Defendants contend that the scan converter operates entirely on a floating point basis. Second, Defendants contend that the scan converter must specify pixels for a display screen. The Court does not find either of these limitations supported by the intrinsic evidence.

Defendants' "floating point" limitation is undermined by the language of Claim 1 of the '158 patent:

> A rendering circuit comprising:
>
> a geometry processor;
>
> a rasterizer coupled to the geometry processor, the rasterizer comprising ***a scan converter*** being configured to scan convert data received at the input, ***at least a portion of the data received at the input being in floating point format***,
>
> the ***scan converter*** being configured to output data from the output, ***at least a portion of the data from the output being floating point data***; and

a frame buffer coupled to the rasterizer for storing a plurality of color values in floating point format.

'158 patent at 12:61-13:5 (emphasis added). According to Claim 1, only a portion of the data being inputted to and outputted from the scan converter needs to be in floating point format.

Similarly, the Court sees no basis for limiting "scan converter" so that it must specify which pixels of the display screen belong to which primitive. The broader construction proposed by Plaintiff, that the "scan converter" "generates pixel and/or fragment positions associated with the primitive" finds some support in the Background Art section of the '158 patent. *See id.* at 1:52-55 ("Many times, portions or 'fragments' of a pixel fall into two or more different primitives. Hence, the more sophisticated computer systems process pixels on a per fragment basis."). Accordingly, the Court will adopt Plaintiff's broader construction.[10]

D. The '145 Patent

1. "large area"

GPH a display area which is actively addressed in an (x, y) matrix of pixels through a thin film transistor array
Defendants Indefinite. To the extent that this term may be construed, it means "having a viewing area measuring 17.3 inches or more diagonally."
Court having a viewing area measuring 135 square inches or more

Defendants contend that the term "large area" relates to the physical dimensions of a display. Plaintiff argues that "large area" instead relates to "pixel dimensions and density." The

[10]The Federal Circuit has construed the term "scan conversion" in relation to the '327 patent. *See Silicon Graphics, Inc.*, 607 F.3d at 790-92. It has not construed "scan converter" in the '158 patent.

Court agrees with Defendant that "large area" relates to the physical dimensions of a display. The Court further finds that the "large area" term is not indefinite because the intrinsic evidence provides a concrete definition for the term. *See Seattle Box Co., Inc. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818, 826 (Fed. Cir. 1984) ("When a word of degree is used the district court must determine whether the patent's specification provides some standard for measuring that degree.").

The only reference to a large area in the patent specification is to 874 square cm (135 square inches) of display area. '145 patent 7:12-14. This measure provides a lower limit for what "large area" means. Defendants propose a construction that converts dimensions of 369.6 mm x 236.54 mm, found at '145 patent 7:10-12, into a diagonal length measurement in inches. However, using a diagonal measurement for defining the area for a viewing screen, though commonly done, finds no support in the specification. Instead, the specification explicitly provides an overall area measurement, and the Court will follow that approach as well.

Plaintiff's construction finds no support in the intrinsic record and does not provide any clarification to the term "large area." The coordinate system through which an area is addressed sheds no light on whether that area is large or small.

2. "optical compensation film"

GPH An optically anisotropic film that increases off-axis viewing angles.
Defendants A birefringent film that compensates for the loss of contrast ratio at off-axis viewing angles created by the liquid crystal layer.
Court An optically anisotropic film that increases off-axis viewing angles.

The primary dispute is whether the optical compensation film must be birefringent, as Defendants contend, or whether it simply needs to be optically anisotropic, which is Plaintiff's position. The specification distinguishes between optical compensation films generally and the more specific birefringent film. *See* '145 patent 9:50-52 ("In one embodiment, birefringence compensation film is used for layer 445 to improve viewing angle."). If the patentees had intended to claim just birefringent film, they could have done so. Instead, the purpose of the optical compensation film, i.e., to increase off-axis viewing angles, may be accomplished by other films that are optically anisotropic.

Defendants argue that Plaintiff's broad construction would read on polarizers, a product that is explicitly distinguished in the patent. However, as Plaintiff points out, although polarizers are optically anisotropic, they do not increase the off-axis viewing angle of a viewing surface. Accordingly, the Court adopts Plaintiff's broader construction.

3. "air gap"

GPH Term should be understood according to its plain and ordinary meaning. To the extent the court determines the construction of the phrase is necessary, GPH proposes the following: A separation between two surfaces filled with air.
Defendants A space between two non-contacting surfaces that is filled with air.
Court A separation between two surfaces filled with air.

The parties' primary dispute with respect to the "air gap" term is whether the two separated surfaces that create the gap must be non-contacting. The Court finds that the air gap does not need to be created by two non-contacting surfaces.

Defendants contend that the surfaces must be non-contacting because the patent

specification, in Figure 7, shows the air gap as being a layer in between two non-contacting surfaces. *See* '145 patent Fig. 7. However, this depiction does not foreclose Plaintiff's broader construction. The figure could have been showing a gap created between two points of contact of the layers adjacent to the gap. Additionally, the extrinsic evidence cited by Defendants is consistent with Plaintiff's position. Defendants cite the Merriam-Webster Dictionary's definition of "gap" as "a hole or space where something is missing." "Gap," *Merriam-Webster.com*, Merriam-Webster (Online Ed.), http://www.merriam-webster.com/dictionary/gap (accessed May 12, 2014). Plaintiff's construction is one that allows for a "hole" or "space" – in between contacting or non-contacting surfaces. Finally, Defendants contend that the patentee disclaimed claim scope when distinguishing the '145 patent from U.S. Patent No. 6,044,196 (the "Winston reference"). However, in traversing that rejection, the patentee distinguished the Winston reference by addressing the location of the air gaps, not the shape or nature of those gaps. (*See* D.I. 185 Ex. 7 at 13-14)

4. "wide aspect ratio"

GPH an aspect ratio greater than 4:3
Defendants an aspect ratio greater than 1.3:1
Court an aspect ratio greater than 1.3:1

The patent specification explicitly states that "[w]ithin the context of the present invention, an aspect ratio greater than 1.3:1 is considered to be a wide aspect ratio." '145 patent, 7:15-21. When an inventor expressly defines a claim in term in the specification, "the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316. Although the specification also states that

VGA, SVGA, XGA, and UXGA standards, each of which has an aspect ratio of 4:3 (1.33:1), are not wide aspect ratios, '145 patent, 1:56-58, these specific disavowals do not overcome the express definition provided by the patentee. *See Sinorgchem Co., Shandong v. Int'l Trade Comm'n*, 511 F.3d 1132, 1138 (Fed. Cir. 2007) ("[V]ague language cannot override . . . express definitional language . . . . When the specification explains and defines a term used in the claims . . . there is no need to search further for the meaning of the term."). Accordingly, the Court will adopt Defendants' well-supported construction.

5. "monitor"

GPH Term should be understood according to its plain and ordinary meaning. To the extent the court determines the construction of the phrase is necessary, GPH proposes the following: "A device that displays graphical information content, including images, text, alphanumeric characters, etc."
Defendants Term should be understood according to its plain and ordinary meaning. To the extent the Court determines the construction of the phrase is necessary, it means "A standalone display device that is separate from and external to the digital computer system/information originating source."
Court No construction necessary.

The term "monitor" only appears in the preamble of the asserted claim. As such, it does not necessarily limit the claim. In fact, "as a general rule[,] preamble language is not treated as limiting." *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1347 (Fed. Cir. 2012). However, "[w]hether to treat a preamble as a limitation is a determination resolved only on review of the entire patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim. No litmus test defines when a preamble limits claim scope."

Poly-Am., L.P. v. GSE Lining Tech., Inc., 383 F.3d 1303, 1309 (Fed. Cir. 2004). Upon reviewing the entire '145 patent, it is clear that the "monitor" language "is not needed to give meaning to the claims, which recite structurally complete inventions without the preamble language." *Id.* The parties agree that the monitor is a display device. Their dispute – whether it needs to be a stand-alone device – need not be resolved by claim construction because "monitor" is not limiting.

6. "digital computer system," "information originating source"

GPH Plain and ordinary meaning
Defendants One or more processing devices that are separate from and external to the monitor.
Court One or more processing devices.

As with the "monitor" term, the parties again dispute whether the "digital computer system" or the "information originating source" must be separate and external to the monitor. Unlike "monitor," the "digital computer system" and "information originating source" terms appear in the text of the claims and are limiting. Defendants support the "separate from and external to the monitor" limitation by referencing the preferred embodiments in the patent. *See, e.g.*, '145 patent Figs. 2-5 (showing monitor as stand-alone device). However, unless a patentee acts as his own lexicographer or disavows claim scope, the Court will not import limitations from a preferred embodiment into the claim. *See Kara Tech. Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1347-48 (Fed. Cir. 2009) ("It is the claims that define the metes and bounds of the patentee's invention. The claims, not specification embodiments, define the scope of patent protection. The patentee is entitled to the full scope of his claims, and we will not limit him to

his preferred embodiment or import a limitation from the specification into the claims."). While Claim 1 recites a "monitor" that comprises "electronic circuitry for receiving signals from a digital computer system," this language does not require the digital computer system to be separate from the monitor. '145 patent 19:50-51. Accordingly, the Court will not import the "separate and external" limitation into these terms and will adopt only the first half of Defendants' construction.

7. "high resolution"

GPH Plain and ordinary meaning. To the extent construction is necessary: "A display resolution that is sufficient to display high information content."
Defendants Indefinite. To the extent that this term may be construed, "a pixel pitch of between 0.22 and 0.26 mm."
Court a pixel pitch of between 0.22 and 0.26 mm

Defendants argue that "high resolution" is indefinite because it has no pre-determined plain and ordinary meaning. Yet Defendants also argue that "at the time of the patent filing, one of ordinary skill in the art would have understood that displays were generally categorized as 'low resolution,' 'medium resolution, 'high resolution,' and 'ultrahigh resolution.'" (D.I. 182 at 15) It seems, then, that "high resolution" did have a pre-defined meaning to one of ordinary skill in the art, and Defendants' expert seems to support this view. (*See* D.I. 183 ¶ 83) (Defendants' expert opining: "[I]f the term 'high resolution' is not indefinite, then the inventor intended 'high resolution' in this patent to mean a pixel pitch between 0.22 and 0.26mm, which is consistent with the definition proposed in the 1992 reference text Handbook of Display Technology by Joe Castellano and the understanding of those of skill in the art when the patent was filed.")

Again, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus*, 134 S. Ct. at 2124. The intrinsic evidence supports Defendants' proffered alternate construction. *See* '145 patent 7:31-38 ("For the display of high information content images, a certain range of pixel pitches is preferred, e.g., between 0.22 mm and 0.26 mm. Below 0.22 mm, the text becomes difficult to read and above 0.26 mm, or so, the images becomes 'pixellated' or 'jaggies' can be seen when diagonal lines are displayed."). Particularly considering Defendants' expert's opinion, the Court concludes that the claims "inform[ed], with reasonable certainty, [one] skilled in the art about the scope of the invention." *Nautilus*, 134 S. Ct. at 2124. Because the patent clearly teaches using a pixel pitch in the 0.22-0.26mm range, and teaches away from using pixel pitches outside that range, the term "high resolution" is not indefinite and the Court will adopt Defendants' construction.

8. "high information content"

GPH Plain and ordinary meaning.
Defendants Indefinite.
Court Indefinite.

Defendants contend that the term "high information content" is indefinite because there is no guidance in the intrinsic record as to what "information content" qualifies as being "high." As already noted, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus*, 134 S. Ct. at 2124. In its recent

Nautilus opinion, the Supreme Court did not disturb the Federal Circuit's prior holding that "[w]hen a word of degree is used[,] the district court must determine whether the patent's specification provides some standard for measuring that degree." *Seattle Box Co.*, 731 F.2d at 826.

Reading the claim in light of the specification, the Court finds that the term "high information content" fails to inform, with reasonable certainty, one of ordinary skill in the art about the scope of the invention. Unlike with "high resolution," there is no standard in the specification for measuring what differentiates "high information content" from "information content" generally. The specification states that "textual information" and "graphic images" may be high information content. '145 patent 7:24-26. However, a person of ordinary skill in the art would be unable to separate textual information and graphic images that contain merely "information content" from text and images that contain "high information content."

Accordingly, the Court finds that the "high information content" term is indefinite.

E. The '389 Patent

1. "gamma profile"

GPH a non-linear relationship between luminosity and input voltage
Defendants an exponential equation defining a brightness curve in the form Vout = Vin^{γ}
Court a non-linear polynomial equation describing any point on a brightness curve

The parties agree that a gamma profile must exhibit a non-linear relationship. They disagree, however, as to whether that relationship must be governed entirely by the function Vout = Vin^{γ}. According to the specification,

> Human eyes see logarithmically. To compensate for this, monitors are made to mimic the eye's viewing so that the display shows the eye information in a way people are used to seeing. The resulting response curve 5 varies in an exponential manner known as the "gamma curve," which is a polynomial equation describing any point on a brightness curve being displayed by a particular monitor.

'389 patent 2:1-8. Both sides cite to this excerpt to support their constructions. In context, the specification uses the terms "gamma curve" and "gamma profile" interchangeably. A gamma curve is "a polynomial equation describing any point on a brightness curve being displayed by a particular monitor." *Id.* Figure 2 shows that the only inputs for determining a gamma profile are Vin and γ. *Id.* at Fig. 2; *see id.* at 6:43-51 (stating in reference to Figure 2 that "[t]he DC reference voltage circuit 240a provides the ON/OFF states of the TFT sub-pixels. The gamma controlling voltage circuit 240b adjusts the DC reference voltages to modify the gamma response of the TFT module 112 without reducing its gray scale resolution. If a new gamma is received and/or determined, it is communicated over bus 250 to the gamma controlling voltages circuit 240b which is used, in part, to implement the desired gamma profile."). Thus, a gamma profile is "a non-linear polynomial equation describing any point on a brightness curve."

2. "gray scale resolution"

GPH a measure of the number of different intensities or shades of gray or color
Defendants total number of steps of intensities (e.g., luminosities) to which each of the red, green, and blue pixels can be driven
Court the degree to which different colors can be achieved by a pixel. It is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.

According to the specification,

> The separate red, green and blue data that correspond to the color intensities of a particular pixel are called the pixel's color data. Color data is often called gray scale data. The degree to which different colors can be achieved by a pixel is referred to as gray scale resolution. Gray scale resolution is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.

Id. at 1:37-44. Thus, the patent defines "gray scale resolution." *See Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301 (Fed. Cir. 1999) (stating that where explicit definition is provided by applicant for term, that definition will control interpretation of term as it is used in claims). The parties have attempted to alter this definition without providing any persuasive justification.

3. "software controller"

GPH a circuit controlled by software
Defendants device operating under control of a software application
Court device operating under control of a software application

The specification states:

> Circuit 240b is coupled to receive control signals over line 250 from a controller device (not shown). In one embodiment, the controller device can be under software control and can be controlled by a host computer.

'389 patent 7:65-8:4. This supports Defendants' construction, whereby the controller device operates under software control. The Court adopts Defendants' proposed construction.

4. "adjustment circuit"

GPH adjustable circuit capable of generating reference voltages
Defendants analog adjustment circuit
Court adjustable circuit that is operable to generate reference voltages

Defendants contend that GPH's construction broadens the scope of the claim by replacing the limitation that the adjustment circuit be "operable" to produce reference voltages to one that need merely be "capable" of doing so. The Court agrees that GPH's construction introduces some ambiguity on this point, so the Court will alter GPH's construction. Defendants' construction, which would require the adjustment circuit to be analog, is not supported by the specification. Accordingly, the Court construes the term "adjustment circuit" as an "adjustable circuit that is operable to generate reference voltages."

F. The '076 Patent

1. "gamma value"

GPH a numeric value used to express a non-linear relationship between luminosity and input voltage
Defendants an exponent value in an exponential equation defining a brightness curve in the form of $Vout = Vin^{\gamma}$
Court an exponent value in an exponential equation defining a brightness curve in the form of $Vout = Vin^{\gamma}$

The parties agree that a gamma value defines the relationship between an input voltage and output luminosity (or voltage). The parties also agree that this relationship is non-linear.

The parties disagree, however, as to whether the "gamma value" in the '076 patent necessarily refers to the gamma in the ideal gamma function $Vout = Vin^{\gamma}$. Figures 11A and 11B, along with the corresponding discussion in the specification ('076 patent col. 14:47-15:25), teach how scalloping and other non-ideal behaviors of the gamma profile can be corrected to approximate the ideal gamma curve. Thus, unlike the '389 patent, the '076 patent discloses an ideal gamma curve. Nothing in the specification alters the understanding of one of ordinary skill in the art that an ideal gamma curve is governed by the function $Vout = Vin^{\gamma}$. Therefore, Defendants' construction most accurately captures the plain and ordinary meaning of the "gamma value" term and will be adopted.

2. "grayscale resolution"

GPH a measure of the number of different intensities or shades of gray or color
Defendants Total number of steps of intensities (e.g., luminosities) to which each of the red, green and blue pixels can be driven.
Court the degree to which different colors can be achieved by a pixel. It is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.

As with the '389 patent, the '076 patent also recites that:

> The separate red, green and blue data that correspond to the color intensities of a particular pixel are called the pixel's color data. Color data is often called gray scale data. The degree to which different colors can be achieved by a pixel is referred to as gray scale resolution. Gray scale resolution is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.

'076 patent at 1:50-59. For the reasons discussed above with respect to the "gray scale

resolution" term in the '389 patent, the Court adopts the same construction for the "grayscale resolution" term in the '076 patent.

3. "backlight control signal"

GPH signal sent to backlight to adjust intensity
Defendants signal sent to backlight to modify color temperature
Court signal sent to backlight to adjust intensity

The '076 patent discloses manipulating a backlight to adjust the intensity of independent lights which, in turn, adjusts the color temperature:

> As discussed above, flat panel backlight control circuitry 575 is responsive to the white balance adjustment control signals to alter a net color temperature of the backlight by independently varying the intensities of light sources 132 and 136 (FIG. 5).

'076 patent at 13:13-17. As the specification notes, the control signal independently varies the intensities of the light sources. These variations, in turn, alter the net color temperature. GPH's construction more accurately captures this meaning. Therefore, the Court will adopt GPH's construction.

4. "graphics controller"

GPH circuit configured to convert image data into RGB data, which is under software control
Defendants a digital processor
Court circuit configured to convert image data into RGB data

The specification teaches:

> In operation, graphics controller 730 receives image data and LUT control signals from processor 12 and converts the image data to appropriate RGB values using graphics rendering engines.

'076 at 14:6-10. Thus, a graphics controller must at least be able to convert image data into RGB data. GPH's construction more accurately captures this meaning – but then it also inserts the unsupported and ambiguous limitation that the controller must be "under software control." Accordingly, the Court adopts GPH's construction but rejects the "under software control" limitation.

5. "image data"

GPH digital data that represents an image
Defendants Plain and ordinary meaning: No construction necessary
Court Plain and ordinary meaning

GPH contends that "image data" can only be digital data. The specification states:

> According to one embodiment of the present invention, the flat panel LCD monitor 216 is configured for coupling to a digital computer system to receive image data to be rendered, and to receive control signals such as white balance adjustment control signals and power management control signals.

'076 patent 12:53-58. GPH uses this and other similar disclosures (*see id.* at 14:6-10) to support the proposition that image data cannot include "a physical picture or a sequence of analog voltages such as would be sent to a CRT." (D.I. 198 at 45) However, sequences of analog voltages are routinely used to transmit digital signals. Because nothing in the specification limits image data to a purely digital format, the Court will not read in the "digital" limitation proposed

by GPH. Instead, the Court agrees with Defendant that "image data" should be given its plain and ordinary meaning.

IV. CONCLUSION

The Court will construe the disputed claim terms of the patents-in-suit consistent with this Memorandum Opinion. An appropriate Order follows.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. ASUS COMPUTER INTERNATIONAL, INC., Defendant.	:	Civil Action No. 12-cv-210-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. TOSHIBA AMERICA INFORMATION SYSTEMS, INC., and TOSHIBA CORPORATION, Defendants.	:	Civil Action No. 12-cv-213-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. VIZIO, INC., Defendants.	:	Civil Action No. 12-cv-214-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. GOOGLE, INC. Defendant.	:	Civil Action No. 12-cv-1394-LPS

GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. HEWLETT-PACKARD COMPANY, Defendant.	:	Civil Action No. 12-cv-1395-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. LENOVO GROUP LTD., et al., Defendants.	:	Civil Action No. 12-cv-1397-LPS
GRAPHICS PROPERTIES HOLDINGS, INC., Plaintiff, v. ASUS COMPUTER INTERNATIONAL, INC., et al., Defendants.	:	Civil Action No. 13-cv-864-LPS

ORDER

At Wilmington this **29th** day of **September, 2014**:

For the reasons set forth in the Memorandum Opinion issued this date, IT IS HEREBY ORDERED that the disputed claim language of U.S. Patent Nos. 6,816,145 ("'145 patent"), 6,650,327 ("'327 patent"), 8,144,158 ("'158 patent), 5,717,881 ("'881 patent"), 6,359,389 ("'389 patent), and 7,136,076 ("'076 patent") shall be construed as follows:

I. UNCONTESTED TERMS

Patent-in-suit	Claim Term	Court's Adopted Construction
'881	an instruction stream of two parcel items in sequence	Plain and ordinary meaning
'327/ '158	rasterization	A graphics operation that translates three dimensional primitives into a set of corresponding fragments and/or pixels and fills them in.
'327/ '158	a rasterization process	One or more of the rasterization processes (e.g., scan conversion, color, texture, fog, shading)
'327/ '158	coupled to	Associated in such a way that power or signal information may be transferred from one to another
'327/ '158	floating point format	A format for representing data by the sign and product of a fraction, or mantissa, and a number raised to an exponent
'327/ '158	s10e5	A 16 bit floating point format composed of one sign bit, ten mantissa bits, and five exponent bits
'327	fragment	A portion of a pixel
'145	light pipe	A structure that takes light from an external source or sources located along the edge or edges of a liquid crystal display and distributes the light across the viewing area of the display

II. CONTESTED TERMS

A. The '881 Patent

Claim Term	Court's Construction
hardwired	the control functions for a digital computer system are generated by hardware using hardware logic design techniques
hardwired supercomputer	A hardwired computer designed to be exceptionally fast and powerful.

instruction fetch means for providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n	Function: Providing an instruction stream of two parcel items in sequence, wherein each two parcel item has a bit length of 2n Structure: Program counter 126 coupled to instruction cache 110 over an address bus.
instruction decode means responsive to each two parcel item for determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits	Function: Responsive to each two parcel item, determining in one clock cycle whether the two parcel item is a single two parcel instruction having a bit parcel instruction having a bit length of 2n bits or two one parcel instructions, each having a bit length of n bits. Structure: The specification does not disclose a corresponding structure, therefore, this limitation is **indefinite** under 35 U.S.C. § 112
one clock cycle	A single period between successive rising edges or successive falling edges of the clock signal used to synchronize the instruction decode means and instruction issue means.
said one clock cycle	*See* "one clock cycle"
instruction issue means responsive to the instruction decode means for issuing each two parcel instruction for execution during said one clock cycle, and for issuing one then the other of the two one parcel instructions for execution in sequence during said one clock cycle and the next succeeding clock cycle	Function: Responsive to the issue decode means, issuing each two parcel instruction for execution during said one clock cycle and issuing one then the other of the two one parcel instructions in sequence during said one cycle and the next succeeding clock cycle Structure: The specification does not disclose a corresponding structure, therefore, this limitation is **indefinite** under 35 U.S.C. § 112.

B. The '327 Patent

Claim Term	Court's Construction
rasterization circuit	An interconnection of specialized electrical hardware for performing rasterization, such as one or more of the processes of scan conversion, assigning colors, lighting, applying texture, applying fog, blending shading, and antialiasing
rasterization process which operates on a . . . floating point format	One of more of the rasterization processes (e.g., scan conversion, color, texture, fog, shading) operate on a floating point format
frame buffer	A portion of computer memory which must store color values and may do so during and/or after rasterization
color values	Attributes of a color (e.g., proportion of red, green, and blue color components)
per-fragment operations	Graphics processing steps within rasterization including one or more of pixel ownership, scissor test, alpha test, stencil test, depth buffer test, dithering, and logic operations.
logic	Hardwired circuitry consisting of logic gates.

C. The '158 Patent

Claim Term	Court's Construction
geometry processor	A processor for performing geometric calculations on a plurality of vertices of a primitive.
scan converter	A subsystem that receives primitives and generates pixel and/or fragment positions associated with the primitive.

D. The '145 Patent

Claim Term	Court's Construction
large area	having a viewing area measuring 135 square inches or more
optical compensation film	An optically anisotropic film that increases off-axis viewing angles.
air gap	A separation between two surfaces filled with air.

wide aspect ratio	an aspect ratio greater than 1.3:1
monitor	No construction necessary.
digital computer system/information originating source	One or more processing devices
high resolution	a pixel pitch of between 0.22 and 0.26 mm
high information content	Indefinite

E. The '389 Patent

Claim Term	Court's Construction
gamma profile	a non-linear polynomial equation describing any point on a brightness curve
gray scale resolution	The degree to which different colors can be achieved by a pixel. It is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.
software controller	device operating under control of a software application
adjustment circuit	adjustable circuit that is operable to generate reference voltages

F. The '076 Patent

Claim Term	Court's Construction
gamma value	an exponent value in an exponential equation defining a brightness curve in the form of $Vout = Vin^{\gamma}$
grayscale resolution	The degree to which different colors can be achieved by a pixel. It is directly related to the amount of different intensities (e.g., luminosities) to which each red, green and blue point can be driven.
backlight control signal	signal sent to backlight to adjust intensity

graphics controller	circuit configured to convert image data into RGB data
image data	Plain and ordinary meaning

UNITED STATES DISTRICT JUDGE