IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

HOME SEMICONDUCTOR CORPORATION, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA INC., SAMSUNG SEMICONDUCTOR INC., and SAMSUNG AUSTIN SEMICONDUCTOR LLC, Defendants.	No. 13-cv-2033-RGA

MEMORANDUM ORDER

Presently before the Court is the issue of claim construction of multiple terms in U.S. Patent Nos. 5,452,261 ("the '261 patent") and 6,146,997 ("the '997 patent"). I have considered the parties' joint claim construction brief. (D.I. 101). I held a *Markman* hearing on February 14, 2019. (D.I. 152).

I. BACKGROUND

The '261 patent relates to a serial address generator for random access memory. '261 patent at 1:6-9. The parties dispute the construction of terms in claims 1, 8-10, and 12-14. The claims provide:

> 1. An address generator for a random access memory, comprising:
>
> > an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; and

an *external address enable switch* connected between an address input terminal of the address generator and the output terminal of the address generator;

wherein the address sequencer includes *means for incrementally timing* the address sequencer to generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the *external address enable switch.*

8. The address generator of claim 1, further comprising *means for providing an externally generated address* to the address input terminal, *wherein* the externally generated address is a first address of a page of the random access memory.

9. An address generator for a random access memory, comprising:

means for providing a first address in a sequence of addresses, *the first address being provided* from an external source as an output address;

an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an output address immediately following *the generation of the first address*;

an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator;

an *external address enable switch* connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for incrementally timing the address sequencer during a preset period to generate the second address at a same time that the first address is being provided from the external source.

10. A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of:

providing from an external source a first address in the sequence as an output address;

switching in the first address as an output address during a preset period;

then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by

incremental timing during at least a part of a duration of the step of providing the first address; and

switching in the second address as an output address after the preset period.

12. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator;

an *external address enable switch* connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series;

wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the *external address enable switch*.

13. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator;

an *external address enable switch* connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address;

wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the *external address enable switch*.

14. An address generator for a random access memory, comprising:

> an address sequencer having a clock input terminal, a preset terminal, and an output terminal;
>
> an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; and
>
> an *external address enable switch* connected between an address input terminal of the address generator and the output terminal of the address generator;
>
> wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the *external address enable switch*, and
>
> wherein the address sequencer includes *a counter having a master portion and a slave portion.*

'261 patent at 7:44-8:4, 8:27-66, 9:3-10:30.

The '997 patent relates to a method of fabricating semiconductor devices, and specifically a method of forming a self-aligned contact hole. '997 patent at 1:6-9. The parties dispute the construction of terms in claims 2 and 9. The relevant claims provide:

1. A method for forming a self-aligned contact hole, comprising the steps of:

> (a) providing a semiconductor substrate having a gate electrode and a *diffusion region* thereon;
>
> (b) forming a conformal layer of etch barrier material overlying the substrate surface including the *diffusion region* and the upper surface and the sidewalls of the gate electrode;
>
> (c) forming an insulating layer overlying the barrier layer;
>
> (d) etching an opening through the insulating layer *self-aligned and borderless* to the *diffusion region* by using the barrier layer as an etch stop; and
>
> (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the *diffusion region* and *simultaneously* forming a spacer of the etch barrier material on the sidewall of the gate electrode.

2. The method as claimed in claim 1, further comprising a step of forming an oxide layer over the *diffusion region* and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

9. A method for forming a self-aligned contact hole, comprising the steps of:

(a) providing a semiconductor substrate having a gate electrode and a *diffusion region* thereon, said gate electrode comprising a capping layer;

(b) forming an oxide layer over the *diffusion region* and on the sidewalls of the gate electrode by thermal oxidation;

(c) forming a conformal layer of silicon nitride overlying the substrate surface including the *diffusion region* and the upper surface and the sidewalls of the gate electrode;

(d) forming an insulating layer overlying the conformal layer of silicon nitride;

(e) etching an opening through the insulating layer *self-aligned and borderless* to the *diffusion region* by using the silicon nitride layer as an etch stop; and

(e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the *diffusion region* and *simultaneously* forming a spacer of silicon nitride on the sidewall of the gate electrode.

'997 patent at 3:54-4:8, 4:26-47.

II. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citation omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324). When construing patent claims, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979–80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification

is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315.

"[T]he words of a claim are generally given their ordinary and customary meaning. . . . [This is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312–13. "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321. "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314.

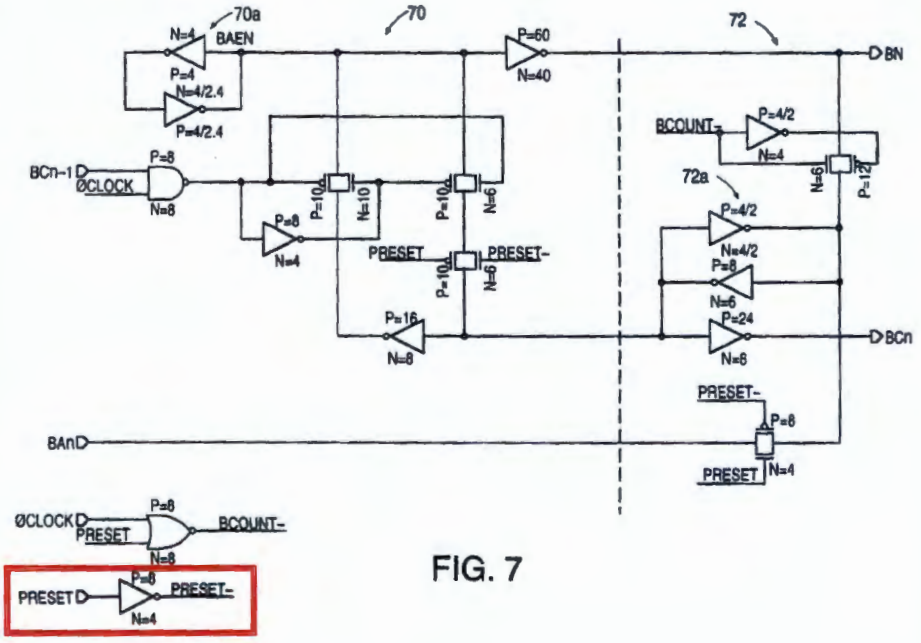
When a court relies solely upon the intrinsic evidence—the patent claims, the specification, and the prosecution history—the court's construction is a determination of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015). The court may also make factual findings based upon consideration of extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317–19. Extrinsic evidence may assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art, and how the invention works. *Id.* Extrinsic evidence, however, is less reliable and less useful in claim construction than the patent and its prosecution history. *Id.*

"A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would

exclude the inventor's device is rarely the correct interpretation." *Osram GMBH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (citation omitted).

III. CONSTRUCTION OF AGREED-UPON TERMS

The Court adopts the following agreed-upon constructions.

Claim Term	Construction
"means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series" ('261 patent, claim 12)	A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6. Claimed Function: during at least a portion of the duration of the first address, providing to the preset terminal a preset signal of predetermined level and duration that sets the address sequencer to the second address in the sequence of addresses Corresponding Structure: the circuitry that produces the timing signal PRESET enclosed in red in Figures 7, 8A, 8B, 9A, 9B, and 10 as shown below:  FIG. 7

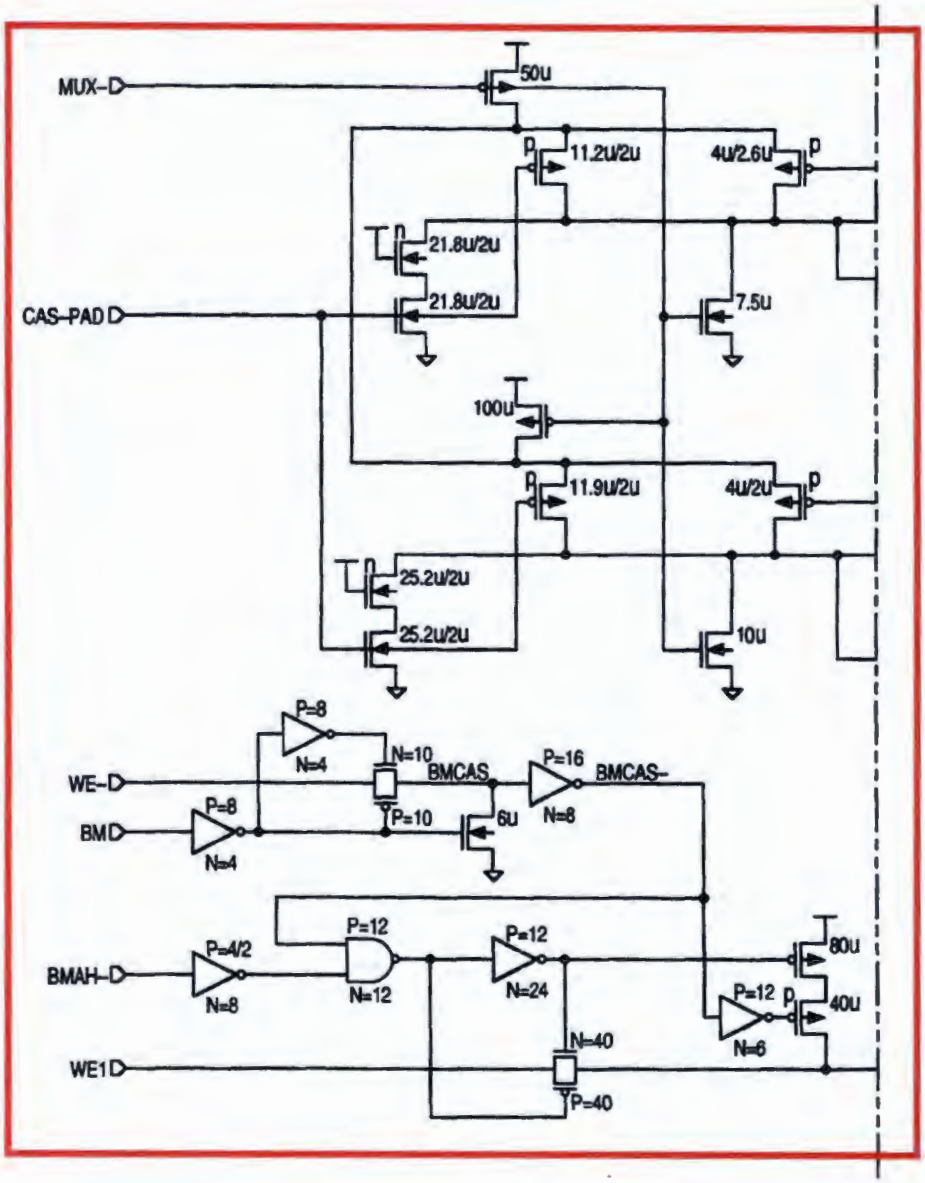
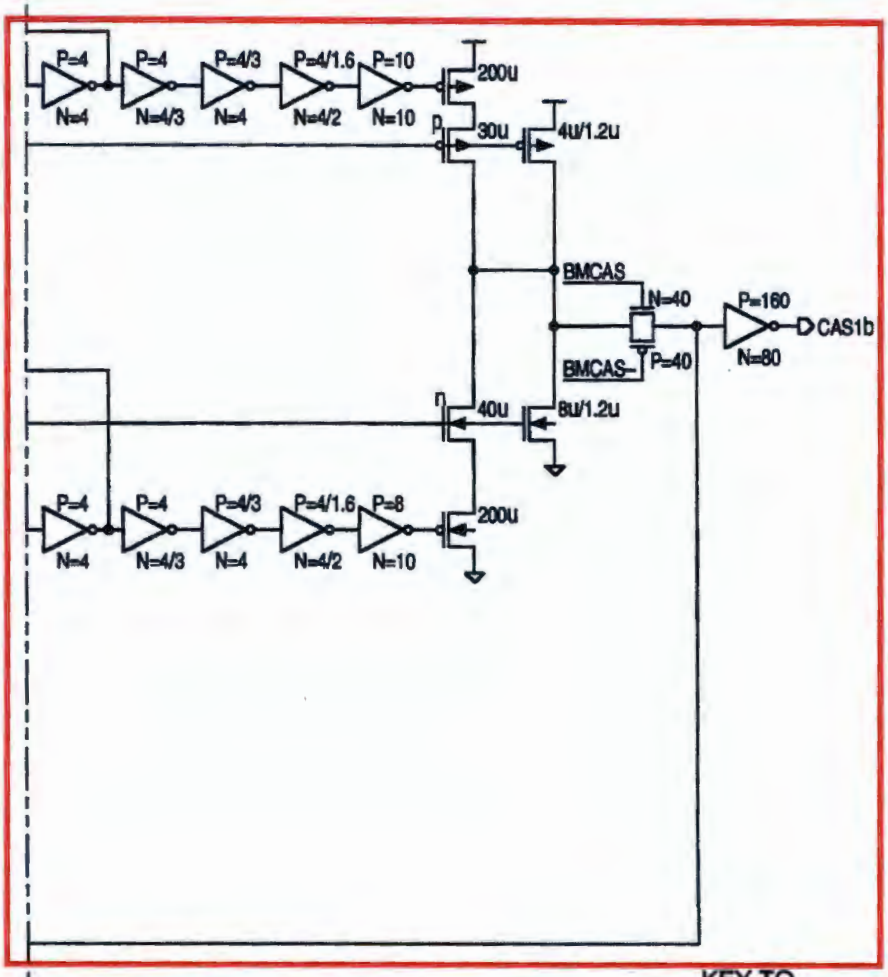
Claim Term	Construction
	

FIG. 8A

Claim Term	Construction
	 FIG. 8B KEY TO FIG. 8 FIG. 8A | FIG. 8B

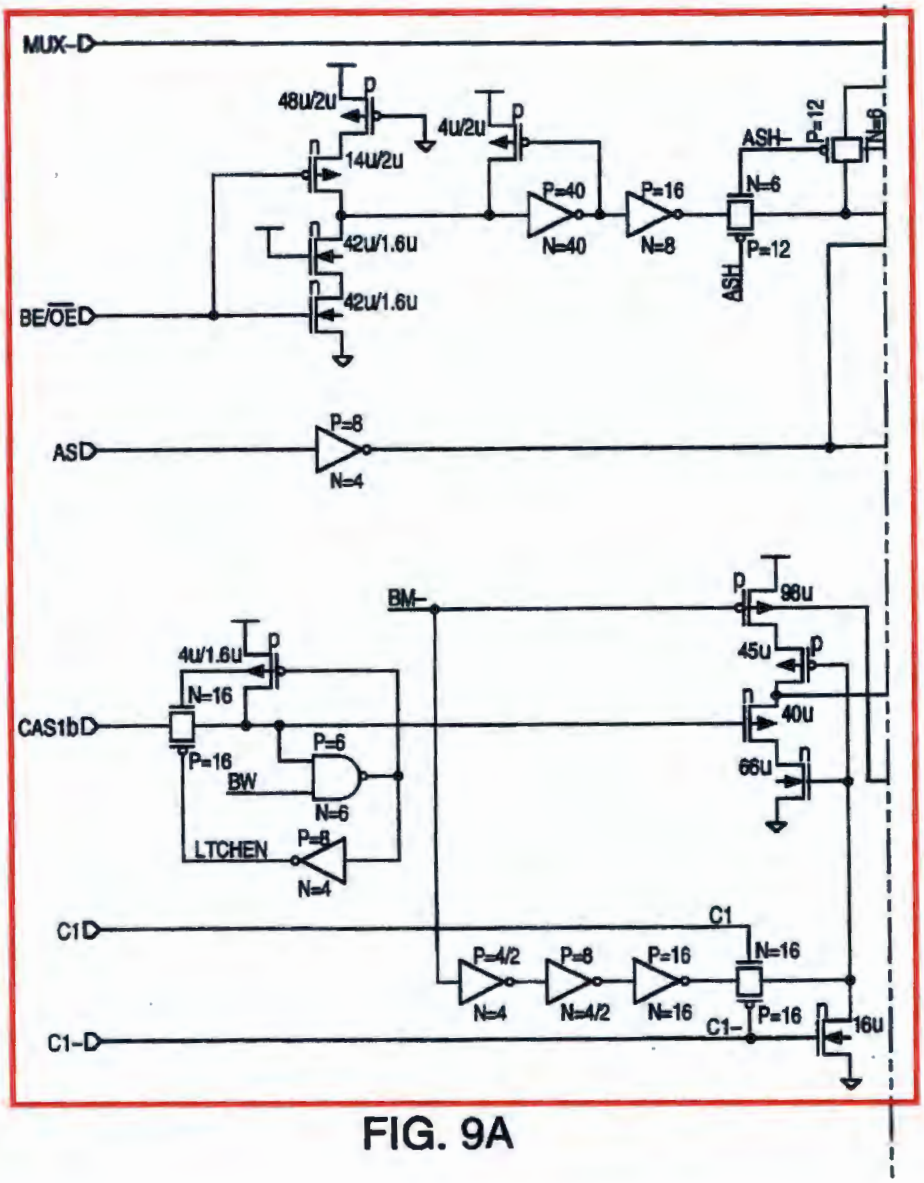
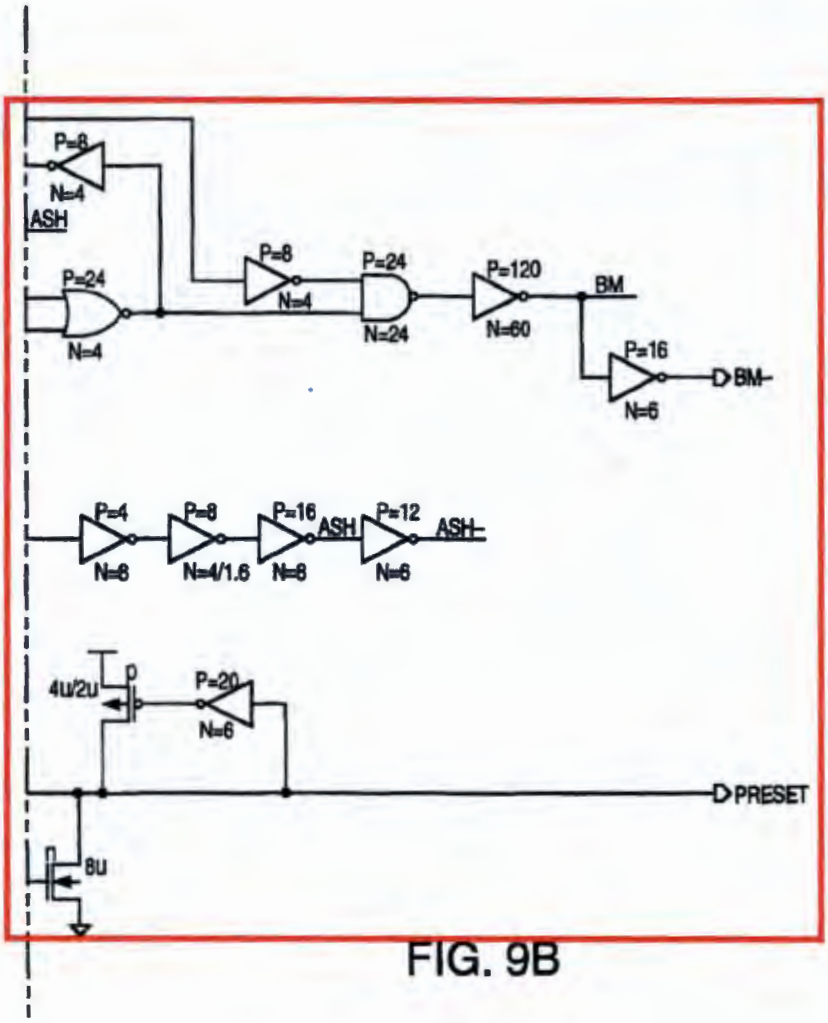
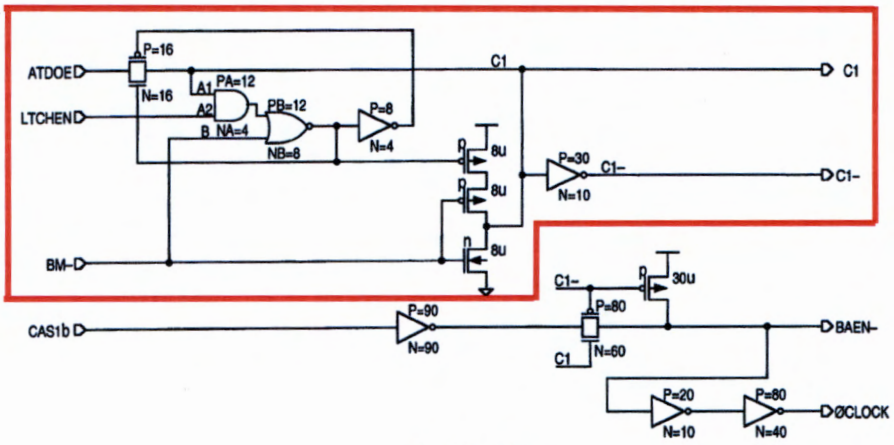
Claim Term	Construction
	

FIG. 9A

Claim Term	Construction
	 FIG. 9B

Claim Term	Construction
	 FIG. 10
"providing first address, switching first address, providing second address, switching second address" ('261 patent, claim 10)	Not indefinite.[1]
"spacer" ('997 patent, claims 2 and 9)	"a structure that spaces between two conductive structures"[2]
"about 100 to 500Å" ('997 patent, claim 11)	Not indefinite.[3]

[1] Samsung withdrew its indefiniteness argument in the joint claim construction brief. (D.I. 101 at 52).

[2] Samsung withdrew its proposed construction in the joint claim construction brief. (D.I. 101 at 87). Therefore, I adopt HSC's construction as the agreed-upon construction. (D.I. 86 at 2).

[3] Samsung withdrew its indefiniteness argument in the joint claim construction brief. (D.I. 101 at 88).

IV. CONSTRUCTION OF DISPUTED TERMS

A. The '261 Patent

1. "means for incrementally timing the address sequencer . . ." (claims 1 and 9); "the second address being generated by incremental timing during at least a part of the duration of the step of providing the first address" (claim 10)

a. Plaintiff's Proposed Construction:

Claimed Function: [i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, A_{n+1} is output within one half clock cycle of A_n.

Corresponding Structure: the circuitry that produces A_{n+1} enclosed in red in Figure 7 as shown below: [4]

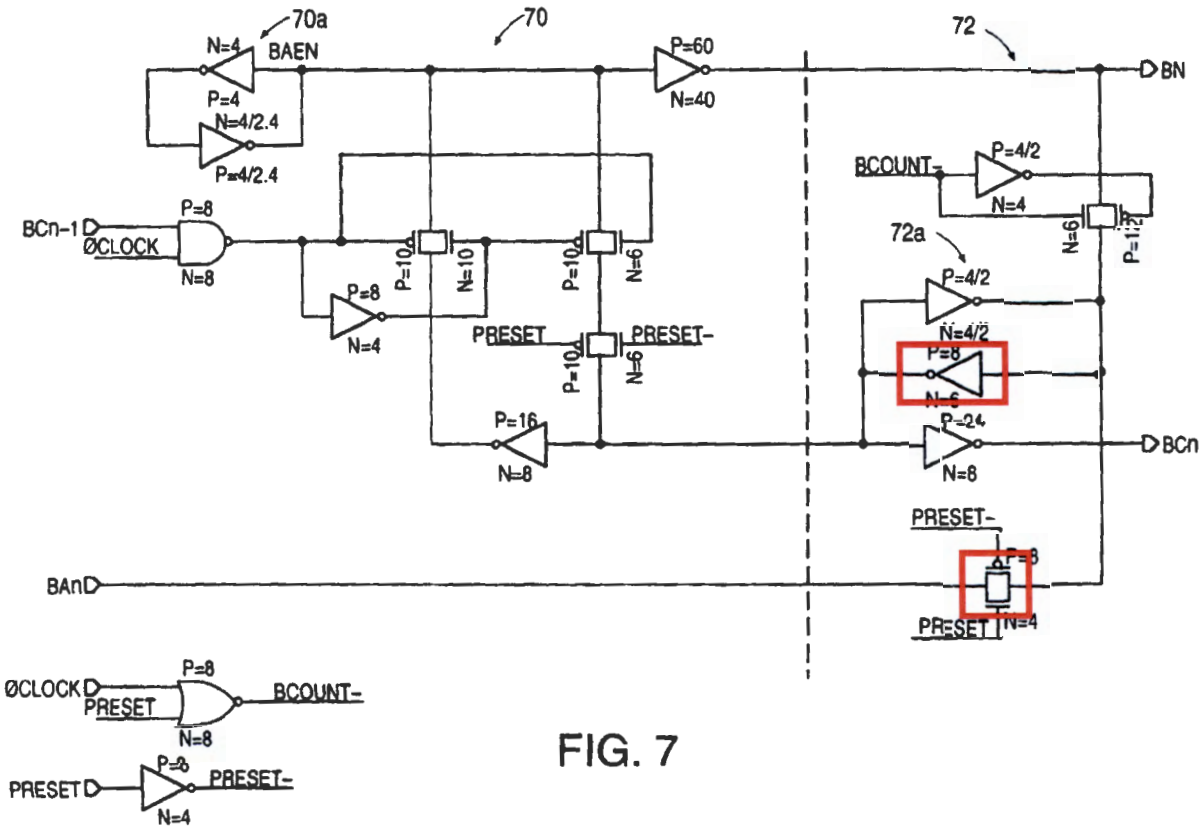


FIG. 7

[4] Figure 7 in the original published patent was replaced with a certificate of correction. (D.I. 102, Ex. A1).

b. Defendants' Proposed Construction:

Claimed Function: [i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, A_{n+1} is output by the address generator within one half clock cycle of A_n.

Or, in the alternative: [i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, the address generator completes outputting A_n and A_{n+1} within one clock cycle from the end of the preset period.

Corresponding Structure: None adequately identified in the specification. At a minimum, Plaintiff's identified structure is incomplete and not adequately linked to the claimed function. Therefore, the means-plus-function limitation is indefinite.

Or, in the alternative: (i) the external address enable switch of Figure 5 to provide the first address A_n as an output address, (ii) the address sequencer of Figure 6 comprising nine cells shown in Figure 7 to produce the second address in the sequence, A_{n+1}, and preset the address sequencer to provide A_{n+1} following A_n, (iii) the internal address enable switch (e.g., as shown in Figure 3 or Figure 5) and circuitry of Figures 8, 9, and 10 to output A_{n+1} by the address generator within one half clock cycle of A_n.[5]

c. Court's Construction:

Claimed Function: [i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, A_{n+1} is output by the address generator within one half clock cycle of A_n.

Corresponding Structure: Not indefinite on the present record. Whether corresponding structure exists and what that structure entails will be determined later when the record is more developed.

The parties agree that § 112, ¶ 6 applies to "means for incrementally timing the address sequencer" in claims 1 and 9. The parties also agree that "the second address being generated by

[5] Defendants identified this alternative structure in a footnote in the joint claim construction brief without further explanation. (D.I. 101 at 21 n.13). It is based entirely on one paragraph of Defendants' expert witness declaration. (D.I. 152 at 37:11-19; D.I. 102, Ex. A7 ¶ 75).

incremental timing during at least a part of the duration of the step of providing the first address" in claim 10, while not a means-plus-function limitation, should be construed according the function portion of the limitation in claims 1 and 9. (D.I. 101 at 5).

Claimed Function (Claims 1 and 9) and Construction (Claim 10)

The parties only dispute part [iii] of the claimed function, which describes the result of the "incremental timing" limitation. The phrase "incremental timing" captures the main benefit of the patented invention, which is an address sequencer that provides an "incremental timing advantage over the prior art." '261 patent at 2:52-58. The specification explains, "[T]he address sequencer generates each address one clock cycle ahead of the time that address would have been generated in the prior art, and the address output is supplied to the output buffer ½ clock cycle ahead of the prior art (FIG. 2B) timing." *Id.* at 2:46-50. To avoid a construction based on the prior art, the parties' proposed functions are based on the timing relationship between the output of the start address A_n and the second address A_{n+1}.

The specification shows that the claimed invention and prior art share the same basic circuitry:

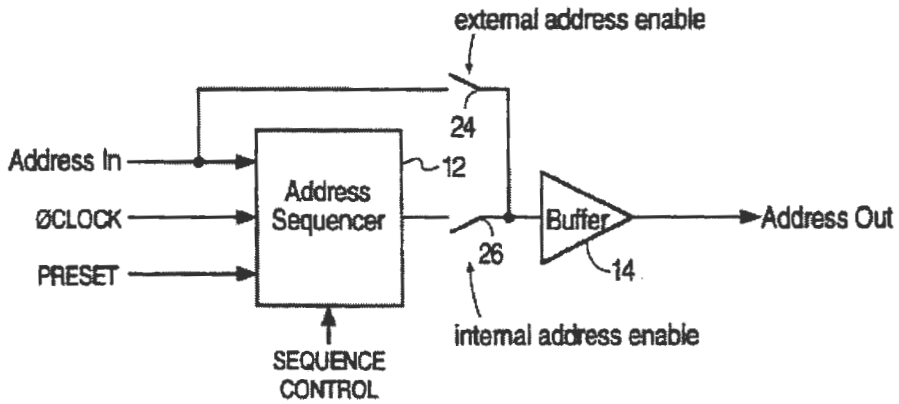


FIG. 1B
(PRIOR ART)

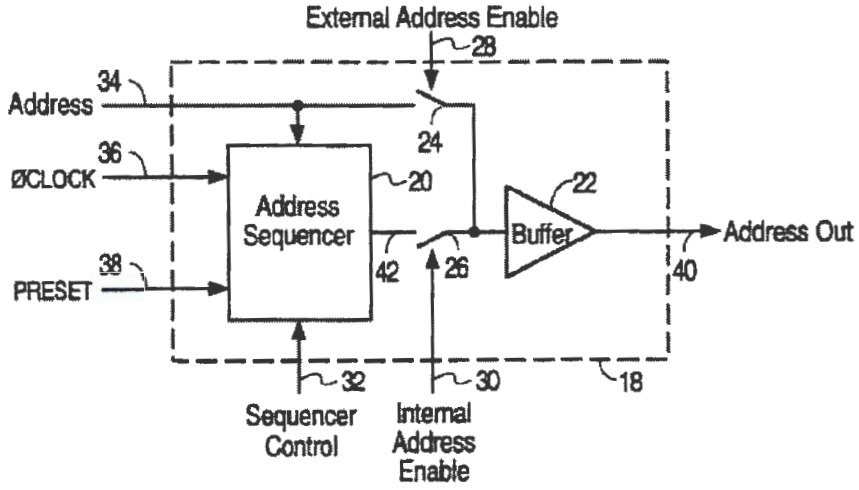


FIG. 3

Initially, the external address enable switch 24 is closed and thus the start address A_n is provided directly to the output buffer (14 in Figure 1B or 22 in Figure 3). *Id.* at 1:65-2:3, 2:18-19. The external address enable switch is then opened, and the internal address enable switch 26 is closed. *Id.* at 2:19-26. As a result, the second address A_{n+1} moves from the address sequencer (12 in Figure 1B or 20 in Figure 3) to the output buffer. *Id.* The improved timing advantage relates to when the second address A_{n+1} is provided by the address sequencer to the output buffer. *Id.* at 2:29-32.

The specification also provides timing diagrams corresponding to the circuits in Figures 1B and 3, which are used to illustrate the claimed timing advantage:

> In the [] described prior art, the second address A_{n+1} is delivered by the address sequencer to the output buffer at the time of the *trailing edge of the first* ϕ_{clock} *cycle*. In accordance with the invention, instead the second address A_{n+1} is delivered to the output buffer at the *leading edge of the* ϕ_{clock} *signal*. Thus one half of a clock cycle is gained for each address burst.

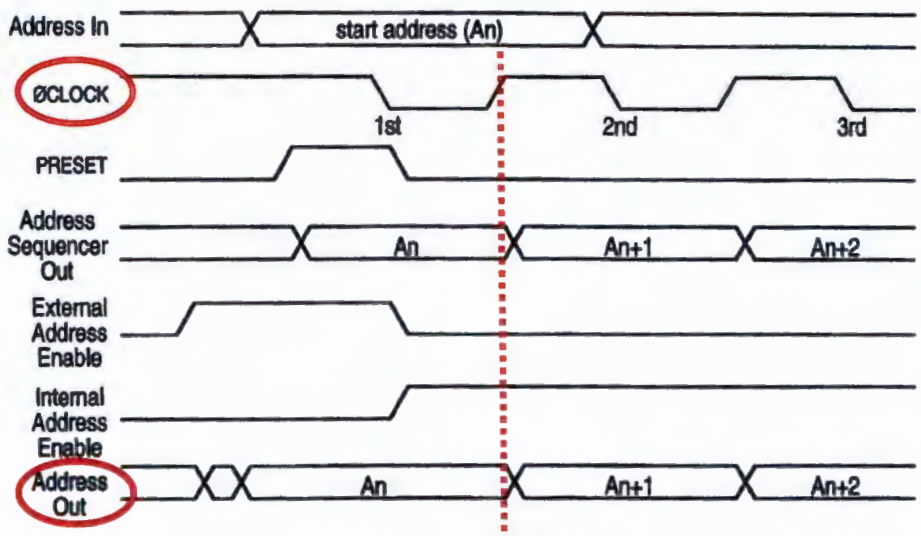


FIG. 2B
(PRIOR ART)

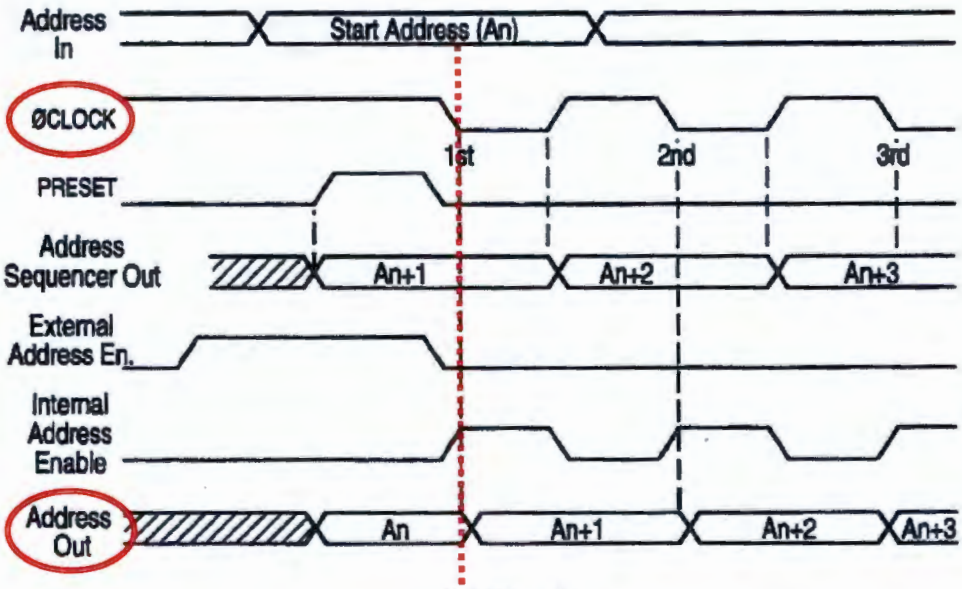


FIG. 4

'261 patent at 2:11-17, Figs. 2B, 4. "Address Out" represents the output buffer (also referred to as output from the address generator). "Address Sequencer Out" represents the address sequencer. "ϕ_{clock}" shows the clock signal, including labels for the start of the first, second, and third clock cycles. As shown above, the specification defines the timing advantage by when

"A_{n+1} is delivered by the address sequencer to the output buffer," which occurs at the "trailing edge" of the first clock cycle in the prior art and the "leading edge" of the first clock cycle in the claimed invention.

Plaintiff's proposed function [iii] states, "as a result, A_{n+1} is output within one half clock cycle of A_n." At the *Markman* hearing, Plaintiff clarified that its construction means A_{n+1} is output from the address sequencer within one half clock cycle of A_n being output from the address generator. (D.I. 152 at 8:13-23). Plaintiff labeled the relevant outputs on Figure 4:

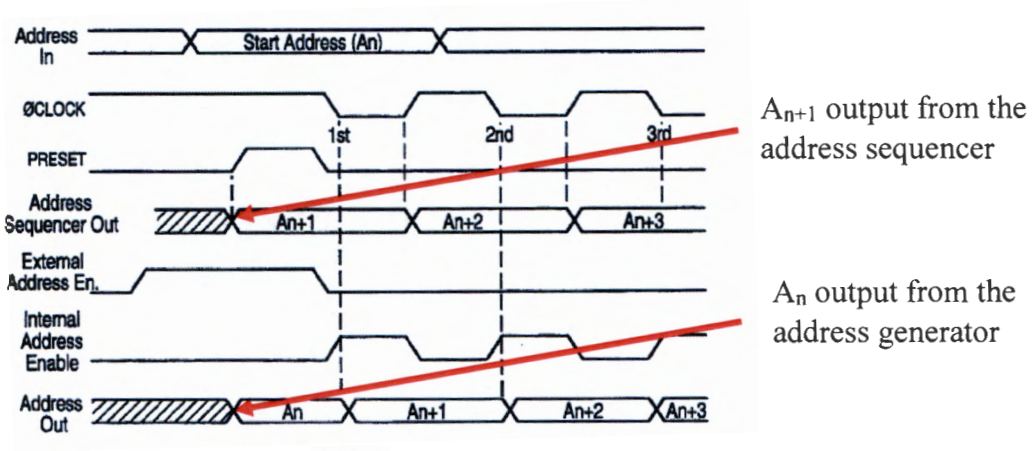


FIG. 4

(*See Markman* Hearing, Plaintiff's slide 20).

I reject Plaintiff's proposed function [iii] as inconsistent with the specification. Plaintiff measures the timing advantage from when A_{n+1} is first output from the address sequencer, before the first clock cycle begins. That is an irrelevant timepoint. The specification makes clear that the address sequencer output is not sampled until the address sequencer receives the first clock signal. '261 patent at 2:40-44. In fact, the internal address enable switch, which connects the address sequencer to the output buffer, is disabled until that first clock signal arrives. *Id.*; *see also id.*, Fig. 3. When the internal address enable switch is disabled, the address sequencer may produce an output, but the output cannot pass to the rest of the circuit. For that reason, the

specification measures the timing advantage from when A_{n+1} is *delivered* from the address sequencer to the output buffer, after the start of the first clock cycle, rather than when A_{n+1} is *first output* from the address sequencer, before the first clock cycle begins. *Id.* at 2:11-17.

Defendants modify Plaintiff's proposed function [iii] to state, "as a result, A_{n+1} is output *by the address generator* within one half clock cycle of A_n." Defendants labeled the relevant outputs on Figure 4:

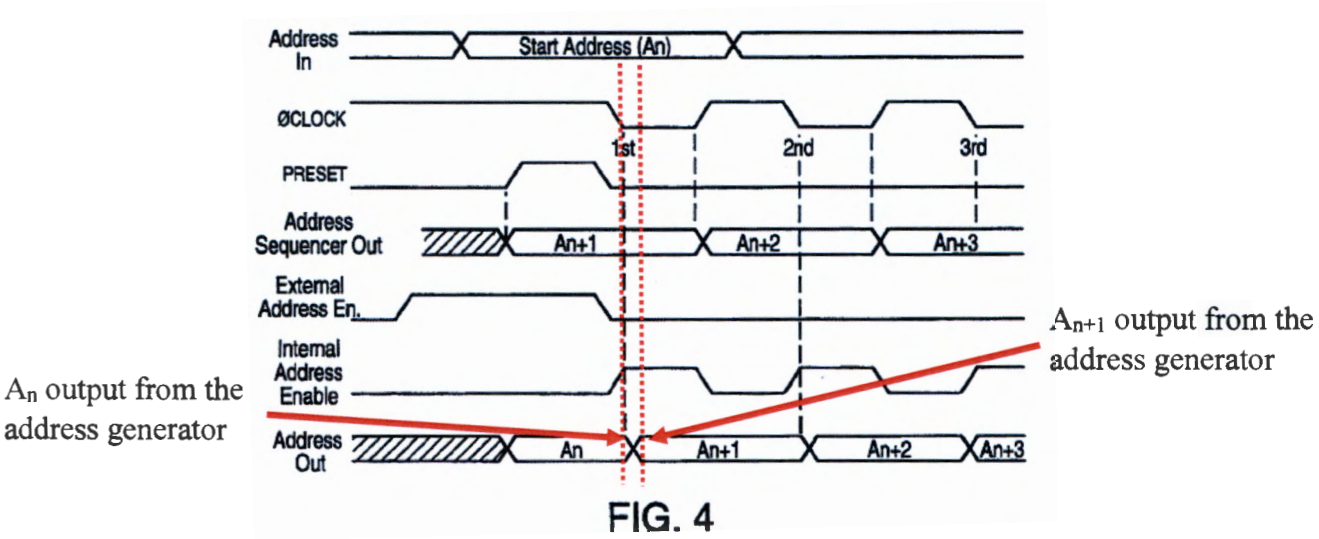


FIG. 4

(*See* D.I. 101 at 15).

Defendants' proposed function [iii] appears to be an accurate reflection of the timing advantage described in the specification. As discussed, the specification provides, "A_{n+1} is delivered [from the address sequencer] to the output buffer at the leading edge of the [first clock cycle]." '261 patent at 2:14-16. A_{n+1} is then output from the output buffer (*i.e.*, the address generator). *See id.*, Figs. 3, 4. As Defendants illustrate in the "Address Out" line of Figure 4, the address generator outputs both A_n and A_{n+1} within the first one half clock cycle. Thus, "A_{n+1} is output by the address generator within one half clock cycle of A_n."

Therefore, I adopt the following as the claimed function of the "means for incrementally timing" limitation (claims 1 and 9) and the construction of the "incremental timing" limitation

(claim 10): "[i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, A_{n+1} is output by the address generator within one half clock cycle of A_n."

Corresponding Structure (Claims 1 and 9)

Plaintiff argues that regardless of which parties' proposed function is adopted, the corresponding structure is the switch and inverter shown in Figure 7. (D.I. 101 at 7-8). Defendants argue that no corresponding structure is identified and thus the "means for incrementally timing" limitation is indefinite. (*Id.* at 17-21). In the alternative, Defendants argue that the corresponding structure is (i) the external address enable switch of Figure 5 to provide the first address A_n as an output address, (ii) the address sequencer of Figure 6 comprising nine cells shown in Figure 7 to produce the second address in the sequence, A_{n+1}, and preset the address sequencer to provide A_{n+1} following A_n,[6] (iii) the internal address enable switch (e.g., as shown in Figure 3 or Figure 5) and circuitry of Figures 8, 9, and 10 to output A_{n+1} by the address generator within one half clock cycle of A_n. (*Id.* at 21 n.13).

As a preliminary matter, the parties disagree on the functions that the corresponding structure must perform. Plaintiff argues that the structure only needs to "incrementally time" the address sequencer. Thus, the structure must allow the address sequencer to be preset to A_{n+1} and to generate A_{n+1} while A_n is provided as an output address, but does not need to actually preset, generate, or output any addresses. (*Id.* at 7-8, 24). Defendants argue that the structure must

[6] The specification explains, "The externally provided address and address out both begin with the same address A_n which is the initial address in the burst, while using the preset signal to advance the counting of the sequence by one count. Therefore, the address sequencer is preset to address A_{n+1} (the second address in the burst) following the externally provide start address A_n." '261 patent at 2:33-39.

provide A_n as an output address, preset the address sequencer to provide A_{n+1} following A_n, and output A_{n+1} from the address generator. (*Id.* at 19-20).

"Where there are multiple claimed functions . . . the patentee must disclose adequate corresponding structure to perform all of the claimed functions." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1351-52 (Fed. Cir. 2015). I identified three claimed functions: "[i] while the first address, A_n, is being provided as an output address, [ii] the second address in the sequence, A_{n+1}, is produced internally by the address sequencer which is preset to provide A_{n+1} following A_n, [iii] as a result, A_{n+1} is output by the address generator within one half clock cycle of A_n. Plaintiff ignores most of the claimed functions. Therefore, Plaintiff's proposed structure is inadequate as a matter of law.

"[S]tructure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). "[I]f a person of ordinary skill in the art would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim, a means-plus-function clause is indefinite." *Williamson*, 792 F.3d at 1352.

Defendants focus their arguments on the alleged deficiencies of Plaintiff's proposed structure. (D.I. 101 at 17-21). In a footnote, Defendants provide an alternative proposed structure based on a single paragraph of their expert's declaration. The expert states, without further explanation:

> [A] person of skill in the art would understand that in order to actually perform the entirety of the claimed function, the corresponding structure would, at minimum, constitute (i) the external address enable switch of Figure 5 to provide the first address An as an output address; (ii) the address sequencer of Figure 6 comprising nine cells shown in Fig. 7 to produce the second address in the sequence, An+1, and preset the address sequencer to provide An+1 following An;

and (iii) the internal address enable switch (e.g., shown as in Fig. 3 and Fig. 5) and circuits of Figs. 8, 9, and 10 to output the second address in a manner that achieves the timing advantage over the prior art.

(D.I. 102, Ex. A7 ¶ 75).

Based on the present record, I cannot find that Defendants have proven indefiniteness by clear and convincing evidence. Defendants' own expert opines that a person of ordinary skill in the art would be able to recognize structure in the specification and associate it with the corresponding claimed function. However, I also cannot find that Defendants' alternative proposed structure is necessarily correct. Defendants propose their structure in a footnote with no accompanying analysis. Therefore, I defer my ruling on corresponding structure to some later point when the record is more developed.[7]

2. "external address enable switch" (claims 1, 9, 12, 13, and 14)

a. Plaintiff's Proposed Construction: Plain and ordinary meaning, which is a switch that connects the first address to the output of the address generator without going through the counters inside the address sequencer.

b. Defendants' Proposed Construction: "a switch that connects the first address to the output of the address generator by bypassing the address sequencer"

c. Court's Construction: "a switch that connects the first address to the output of the address generator by bypassing the address sequencer"

The parties agree that the "external address enable switch" is switch in the claimed address generator that allows the first address to bypass at least some part of the address sequencer. The issue for claim construction is whether the first address bypasses the entire address sequencer or merely the counters inside the address sequencer. (D.I. 101 at 31, 33).

[7] The parties should meet and confer and jointly propose a course for resolving this issue.

As a preliminary matter, Plaintiff argues that "external address enable switch" is just a "typical" switch and thus does not require construction. (D.I. 101 at 30). Plaintiff proposes a specific construction under the guise of the plain and ordinary meaning. The parties clearly dispute the scope of "external address enable switch." Thus, I will construe the term such that I resolve the parties' dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008).

Defendants argue that the specification supports finding the "external address enable switch" as bypassing the entire address sequencer. (D.I. 110 at 31-33). The '261 patent specification discusses the "external address enable switch" in Figures 1B and 3. As discussed, Figure 1B shows a prior art circuit while Figure 3 shows an embodiment of the claimed invention. The specification states, "[T]he address sequencer 12 of FIG. 1B is bypassed before and during the preset period by means of external address enable switch 24 . . . and the start address is provided directly to the output buffer via external address enable switch 24." '261 patent at 1:65-2:3. The specification describes the prior art address sequencer as "typically a counter." *Id.* at 1:21-22. Figure 3 includes the same "external address enable switch 24 (as in FIG. 1B)." *Id.* at 3:28-34. However, Figures 1B and 3 differ "in the internal structure and operation" of their respective address sequencers. *Id.* at 3:35-40.

Figures 5 and 6 provide a more detailed look at the components of Figure 3. Figure 5 shows one of nine identical units that would be used in Figure 3—one unit for each address bit in a nine bit address output signal. *Id.* at 5:62-68. The "external address enable switch" 24 from Figure 3 is labeled as switch 50 in Figure 5. *Id.* at 6:4-6. Figure 6 shows "the counter (corresponding to the address sequencer 20 of FIG. 3)." *Id.* at 6:33-34. "[T]he counter of FIG. 6 occurs only once in the address sequencer 20 and services all nine address buffer circuits, of

which only one is shown in FIG. 5." *Id.* at 6:45-48. Figure 5 does not show the address sequencer 20 or its counters. *See id.* at 6:7-15, Figs. 5A, 5B (explaining that the signal "BN," which is shown entering Figure 5A, comes from the counter in Figure 6).

Nothing in the specification indicates that the "external address enable switch" is specific to the counters inside the address sequencer.[8] Rather, in all the described embodiments, the "external address enable switch" is outside the address sequencer, meaning it would bypass the entire address sequencer. While it is true that claims are not limited to the specific embodiments in the specification, courts may rely on those embodiments to determine how a person of ordinary skill in the art would have understood the claim term. *Phillips*, 415 F.3d at 1323-24.

Plaintiff argues that the "external address enable switch" should only require bypassing the counters inside the address sequencer because the specification describes the counters as a source of delay in the prior art. (D.I. 101 at 31). The specification compares two prior art circuits. Figure 1A "delivers the first address late, due to the propagation delay through the counters inside the address sequencer." '261 patent at 1:55-58. Figure 1B "improve[s] the start address delivery" by providing the start address "from the Address Input directly, instead of going through the counters." *Id.* at 1:60-65.

I do not find Plaintiff's argument persuasive. The fact that bypassing the counters in the address sequencers provided a timing benefit in the prior art does not mean that the "external address enable switch" must be limited to only bypassing the counters. The same benefit would be achieved by bypassing the entire address sequencer. Further, the specification explicitly states that the claimed invention, at least in Figure 3, differs from the prior art "in the internal

[8] Defendants also argue that the specification uses "address sequencer" and "counters" interchangeably. (D.I. 101 at 33). I disagree. Although the specification focuses on the counters, it implies that the counters are a separate component within the address sequencer. *E.g.*, '261 patent at 6:45-48 (describing the counter as occurring in the address sequencer).

structure and operation" of its address sequencer. *Id.* at 3:35-40. Therefore, there is no guarantee that bypassing the counters in the prior art will have the same effect in the claimed invention.

Viewing the specification as a whole, I believe a person of ordinary skill in the art would conclude that the "external address enable switch" bypasses the entire address sequencer. The specification gives no indication that the term should be further limited to only bypass the counters inside the address sequencer. All references to the bypass refer to the address sequencer generally. Therefore, I adopt Defendants' proposed construction.

3. "a counter having a master portion and a slave portion" (claim 14)

a. Plaintiff's Proposed Construction: Plain and ordinary meaning, which is a counter having a master side and a slave side.

b. Defendants' Proposed Construction: "a counter having a first side that holds a value and a second side that holds a value"

c. Court's Construction: Plain and ordinary meaning, which is a counter having a master side with one value and a slave side with a second value.

The specification describes the claimed invention as having "a master/slave counter," wherein "the master side" is initially set to one value and "the slave side" is initially set to a second value. '261 patent at 2:52-56. A master-slave relationship is a term of art with a known meaning. (D.I. 101 at 36; D.I. 152 at 71:3-5). The parties' only dispute relates to the structure of the master/slave counter. The parties agree that the master side and slave side each have a value but disagree over whether some structure must exist to "hold" those values. (D.I. 101 at 36-37; D.I. 152 at 69:18-23, 73:4-14).

Defendants seek to add a structural limitation to the plain and ordinary meaning of "a counter having a master portion and a slave portion." The specification only states that each portion is initially set to a value. '261 patent at 2:52-56. It does not require the master/slave

counter to have any particular structure that holds those values. Defendants' only evidence to the contrary is Figure 7, which shows a latch that holds a value on each side of the counter. (D.I. 101 at 36-37). Figure 7 is merely a preferred embodiment, however, and is not necessarily limiting. *Phillips*, 415 F.3d at 1323.

I do not think the specification supports limiting "a counter having a master portion and a slave portion" beyond its plain and ordinary meaning. The parties' only dispute is whether a circuit can meet that plain and ordinary meaning if it does not have a structure that holds a value on each side of the counter. (D.I. 152 at 76-4-77:3). That is a question of fact to be addressed through expert testimony. Therefore, I construe "a counter having a master portion and a slave portion" as its plain and ordinary meaning, which is "a counter having a master side with one value and a slave side with a second value."[9]

4. "means for providing an externally generated address[, wherein the externally generated address is a first address of a page of the random access memory]" (claim 8)

a. Plaintiff's Proposed Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing an externally generated address to the address input terminal.

[9] Plaintiff agreed that this construction is correct. (D.I. 152 at 69:18-23).

Corresponding Structure: the circuitry that provides the signal to the address input terminal enclosed in red in Figure 5A as shown below:

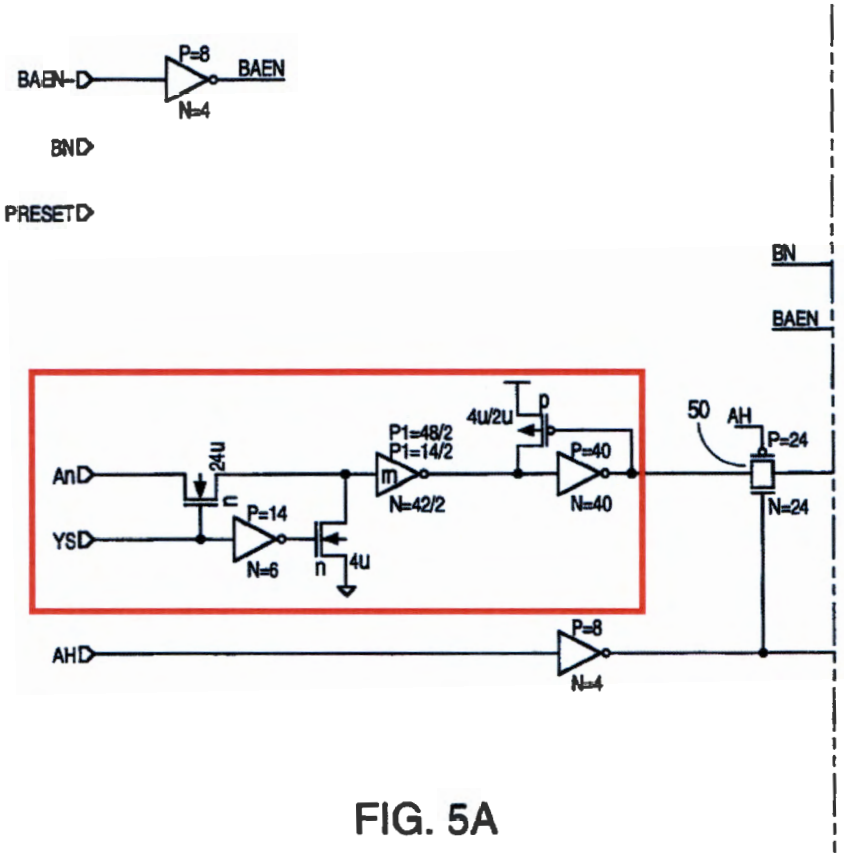


FIG. 5A

b. Defendants' Proposed Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory.

Corresponding Structure: a host computer or processor.

c. Court's Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory.

Corresponding Structure: a host computer or processor.

Claim 8 provides, "The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory." '261 patent at 8:27-31. The parties agree that § 112, ¶ 6 applies, but disagree on whether the relevant limitation includes the portion of the claim following "wherein."

Claimed Function

The only dispute over function is whether the "wherein" clause is part of the claimed function.

Defendants argue that, under *Lockheed Martin Corp. v. Space Sys./Loral, Inc.*, 324 F.3d 1308 (Fed. Cir. 2003), the "wherein" clause can only be excluded from the claimed function if it describes a "result," which it does not. (*Id.* at 41). While I do not think *Lockheed Martin* controls, I agree that it is relevant. In *Lockheed Martin*, the disputed portion of the claim provided:

> [M]eans for rotating said wheel in accordance with a predetermined rate schedule which varies sinusoidally over the orbit at the orbital frequency of the satellite *whereby* the attitude of said satellite is offset in response to the effect of said rotating wheel by the direction of the pitch axis being changed with respect to said momentum vector, the direction of said pitch axis with respect to the inclined orbit normal varying sinusoidally at the orbital frequency to null said roll pointing error due to said orbit inclination, the momentum vector being maintained perpendicular to the plane of the geo-synchronous orbit to null said yaw pointing error due to said orbit inclination.

Id. at 1315. The court excluded the "whereby" clause from the claimed function because it "merely states the result of the limitations in the claim." *Id.* at 1319. In contrast, the "wherein" clause here does not describe the result of the "means for providing" limitation. Rather, it describes the features of the externally generated address to be provided.

In another "whereby" case, the Federal Circuit held, "[W]hen the 'whereby' clause states a condition that is material to patentability, it cannot be ignored in order to change the substance

of the invention." *Hoffer v. Microsoft Corp.*, 405 F.3d 1326, 1329 (Fed. Cir. 2005). The court found the "whereby" clause described a capability that was "more than the intended result of a process step," but "part of the process itself." *Id.* at 1330. The court further cited to the specification and prosecution history that described the whereby element as "an integral part of the invention." *Id.*

Plaintiff argues that here, in contrast to *Hoffer*, the specification and prosecution history never identified the "wherein" clause as integral to the claimed invention. Therefore, the "wherein" clause is not material to patentability and should not be included in the claimed function. (D.I. 101 at 43-44). Plaintiff overstates the holding in *Hoffer*. I do not think *Hoffer* requires every clause in a claimed function to be supported by explicit intrinsic evidence that the clause is integral to the claimed invention.

"The function of a means-plus-function claim must be construed to include the limitations contained in the claim language." *Lockheed Martin*, 324 F.3d at 1319. It is undisputed that the claimed function of "means for providing an externally generated address" includes providing an externally generated address. The "wherein" clause describes limitations of that externally generated address. Plaintiff's proposed construction, by excluding that description, improperly reads out limitations in the claim language. Therefore, I adopt Defendants' proposed claimed function, which includes the "wherein" clause limitations.

Corresponding Structure

Plaintiff argues that for either proposed claimed function, the corresponding structure is that shown in Figure 5A. (D.I. 101 at 39). Plaintiff identifies no part of the specification or prosecution history linking Figure 5A to the claimed function. (*Id.* at 39-40); *B. Braun*, 124 F. 3d at 1424. Therefore, I reject Plaintiff's proposed structure.

Defendants argue that the only structures linked in the specification to the function of "providing an externally generated address" are a host computer or processor. (*Id.* at 42). I agree. The specification states, "Typically the start address of a particular address burst is provided from an external source (a host computer or a processor) . . . ." '261 patent at 1:15-18.[10] Therefore, I adopt Defendants' proposed corresponding structure.

5. "means for providing a first address in a sequence of addresses[, the first address being provided from an external source as an output address]" (claim 9)

a. Plaintiff's Proposed Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing a first address in a sequence of addresses.

Corresponding Structure: the circuitry that provides the signal to the address input terminal enclosed in red in Figure 5A as shown below:

[10] Although the specification was describing the prior art, I believe the claimed invention uses the same structure. The specification indicates that the claimed invention only differs from the prior art with respect to the address sequencer, which is not involved in providing an externally generated address. '261 patent at 2:11-26, 2:63-3:2, 3:35-10.

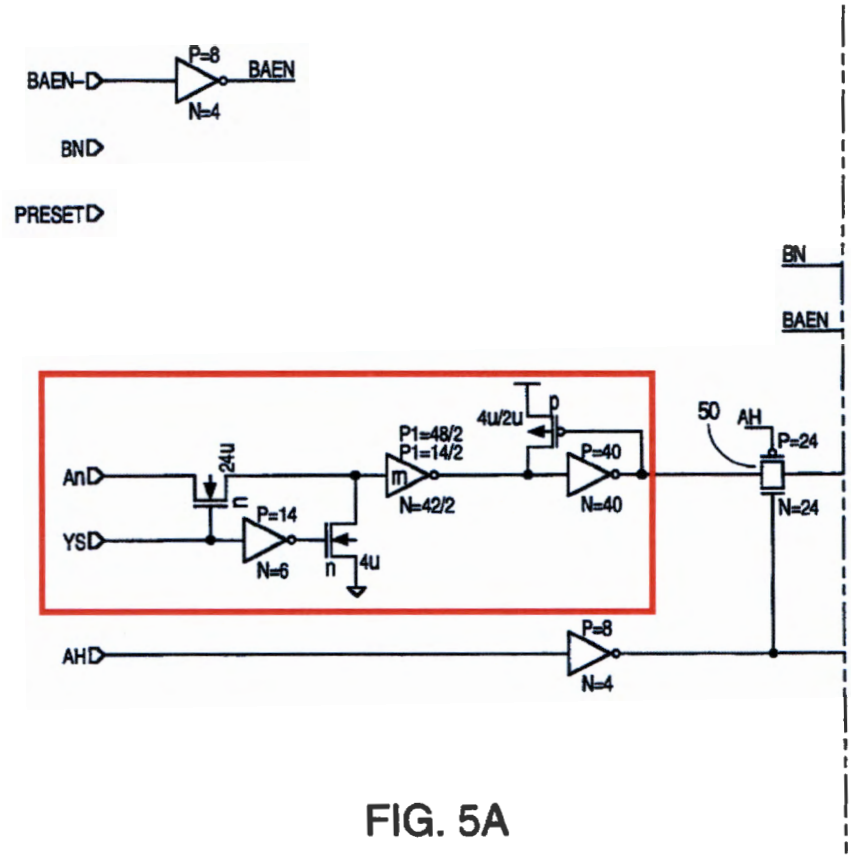


FIG. 5A

b. Defendants' Proposed Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing a first address in a sequence of addresses from an external source as an output address.

Corresponding Structure: a host computer or processor.

c. Court's Construction: A means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

Claimed Function: providing a first address in a sequence of addresses from an external source as an output address.

Corresponding Structure: a host computer or processor.

Claim 9 states in relevant part, "[M]eans for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address." '261 patent at 8:34-36. Again, the parties agree that § 112, ¶ 6 applies, but disagree on whether the

limitation includes the portion of the claim after the comma. The parties' dispute is analogous to that over the claim 8 limitation. (D.I. 101 at 46-48). Although the second clause here does not begin with "wherein," it serves the same purpose as the "wherein" clause in claim 8—describing limitations of the first address to be provided. The parties also make the same arguments for corresponding structure. (*Id.*). Therefore, for the reasons discussed with respect to claim 8, I adopt Defendants' proposed claimed function and corresponding structure.

6. "the generation of the first address" (claim 9)

a. Plaintiff's Proposed Construction: Not indefinite.

b. Defendants' Proposed Construction: Indefinite.

c. Court's Construction: Not indefinite on the present record.

The parties dispute whether "the generation of the first address" is indefinite for lack of antecedent basis. As discussed, claim 9 includes a means-plus-function limitation for "*providing*" a first address. The claim also requires "an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an output address immediately following the *generation* of the first address." '261 patent at 8:37-41. Therefore, "the generation of the first address" has no explicit antecedent basis.

"[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). The absence of explicit antecedent basis is not dispositive. The relevant question is whether, despite that absence, "the scope of a claim would be reasonably ascertainable by those skilled in the art." *Energizer Holdings, Inc. v. Int'l Trade Comm'n*, 435

F.3d 1366, 1370 (Fed. Cir. 2006) (quoting *Slimfold Mfg. Co. v. Kinkead Indus., Inc.*, 810 F.2d 1113, 1116 (Fed. Cir. 1987)); *see also In re Downing*, 754 F. App'x 988, 996 (Fed. Cir. 2018).

Defendants argue that providing and generating are not the same thing, as evidenced by the plain meaning of the words. Therefore, "generation of the first address" cannot derive antecedent basis from "means for providing a first address." (*Id.* at 49-50).

Plaintiff argues that a person of ordinary skill in the art would understand the use of "generation" to be a typo. Instead, the claim element would be read as "following the [provision] of the first address." (*Id.* at 49 & n.18, 51). Plaintiff asserts that the specification repeatedly shows that the second address is provided as an output address following the provision of the first address. For example, the specification states, "After provision to the output buffer of the first address A_n (which is externally supplied as in FIG. 1B) . . . the address sequencer [is allowed] to provide the subsequent internally generated address A_{n+1} to the output buffer." '261 patent at 2:18-29; *see also id.* at 3:58-64 ("After the initial address A_n (which is externally provided) is provided to [the output buffer], . . . the address sequencer [] has generated the second address A_{n+1}.").

"A district court can correct a patent only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims." *Rembrandt Data Techs., LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011) (quoting *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1357 (Fed. Cir. 2003)). "Those determinations must be made from the point of view of one skilled in the art." *Ultimax Cement Mfg. Corp. v. CTS Cement Mfg. Corp.*, 587 F.3d 1339, 1353 (Fed. Cir. 2009)).

At this point, it is unclear whether a person of ordinary skill in the art would find that changing "generating" to "providing" is a minor correction free from "reasonable debate" and evident from the prosecution history. Therefore, based on the present record, I find that Defendants have failed to show indefiniteness by clear and convincing evidence.

B. The '997 Patent

1. "simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode" (claim 2); "simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode" (claim 9)

a. Plaintiff's Proposed Construction: "anisotropic etching of the barrier layer also forms a spacer of etch barrier material on the sidewall of the gate electrode" (claim 2); "anisotropic etching of the silicon nitride layer also forms a spacer of silicon nitride on the sidewall of the gate electrode" (claim 9)

b. Defendants' Proposed Construction: "the spacer is made from the conformal layer of etch barrier material formed in step (b) without additional deposition and etch steps to form the spacer" (claim 2); "the spacer is made from the conformal layer of silicon nitride formed in step (c) without additional deposition and etch steps to form the spacer" (claim 9)

c. Court's Construction: "anisotropic etching of the barrier layer also forms, in the same process step, a spacer of etch barrier material on the sidewall of the gate electrode" (claim 2); "anisotropic etching of the silicon nitride layer also forms, in the same process step, a spacer of silicon nitride on the sidewall of the gate electrode" (claim 9)

Claim 9 is a multi-step method for fabrication of semiconductor devices. The last step states, "anisotropically etching[11] the silicon nitride layer underneath the opening [etched in the prior step], thereby exposing the diffusion region and *simultaneously* forming a spacer of silicon nitride on the sidewall of the gate electrode." '997 patent at 4:44-47.[12] The parties agree that "simultaneously" requires the anisotropic etching and the formation of the spacer to occur in a

[11] Anisotropic etching preferentially etches in the vertical direction. (D.I. 101 at 53 n.20).

[12] Claim 2 has an analogous limitation that replaces "silicon nitride" with "etch barrier material." As the same analysis applies to both claims, I will only address claim 9.

single process step. (D.I. 101 at 53, 56-57). Defendants argue, however, that Plaintiff's construction would broaden the claim to incorporate the prior art. Thus, Defendants propose a construction with an explicit negative limitation to exclude any additional deposition or etch steps to form the spacer. (*Id.* at 53). Plaintiff argues that Defendants misconstrue the prior art. (*Id.* at 57).

The specification describes a "conventional" prior art method in detail. That method requires two layers of silicon nitride, which are deposited and etched in separate steps.[13] The method starts with a semiconductor substrate having gate electrodes each capped with an insulator 16. The substrate is covered with oxide layer 20 (shown in blue) and the first silicon nitride layer 22 (shown in red). '997 patent at 1:24-31, 32-35, Fig. 1B. Silicon nitride layer 22 is anisotropically etched to form the sidewall spacers 22a (also shown in red). *Id.* at 1:35-8, Fig. 1C.

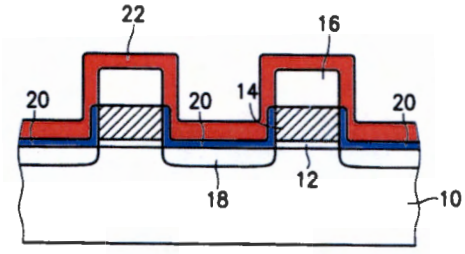


Fig. 1B (Prior Art)

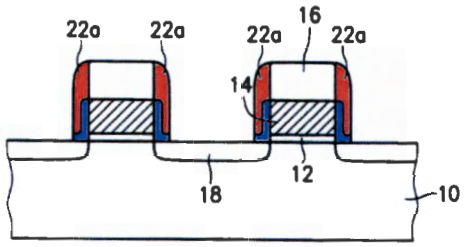


Fig. 1C (Prior Art)

Oxide layer 20 is then removed to expose the diffusion region 18. *Id.* at 1:38-40. The second silicon nitride layer 24 (shown in green) is deposited, covering the diffusion region 18 and sidewall spacers 22a. Layer 24 is then covered by the insulating layer 26. *Id.* at 1:41-46, Fig. 1D. The contact hole 29 (*i.e.*, the "opening") is etched in the insulating layer 26. Silicon nitride layer 24 acts as an etch stop, protecting the diffusion region 18. *Id.* at 1:50-52, Fig. 1E.

[13] The second layer is "etch barrier material," which is "typically" silicon nitride. '997 patent at 1:41-4.

After the contact hole 29 is formed, layer 24 is etched to expose the underlying diffusion region 18. *Id.* at 1:52-53, 64-65, Fig. 1E.

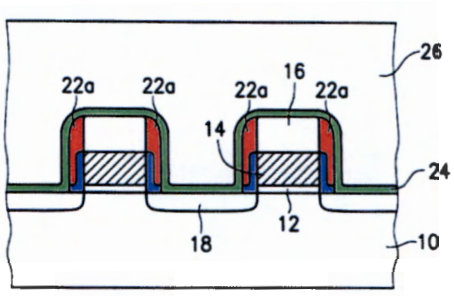


Fig. 1D (Prior Art)

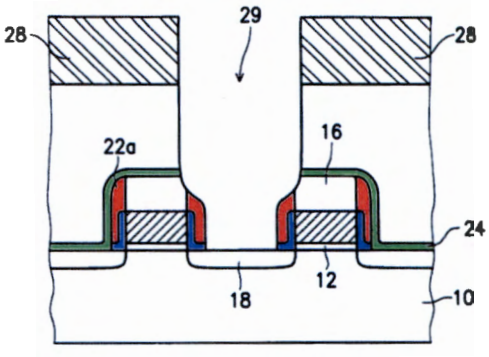


Fig. 1E (Prior Art)

In contrast, the claimed invention only requires a single layer of silicon nitride, which acts as an etch stop during the contact hole etching and is used to form the sidewall spacers. *Id.* at 2:62-65. The claimed method begins with the same substrate covered with an oxide layer 60 (shown in blue). *Id.* at 2:48-59, Fig. 2A. The silicon nitride layer 62 (shown in red) is deposited over the oxide layer and covered by an insulating layer 64. *Id.* at 2:60-3:2 Figs. 2B, 2C. The contact hole 67 is etched in the insulating layer 64. The silicon nitride layer 62 acts as an etch stop, protecting the diffusion region 58. *Id.* at 3:10-14. After the contact hole 67 is formed, the silicon nitride layer 62 is anisotropically etched to remove the portion over the diffusion region 58 and simultaneously form the sidewall spacers 62a (also shown in red). *Id.* at 3:17-21, Fig. 2D. Oxide layer 60 is then removed to expose the diffusion region 58. *Id.* at 21-24, Fig. 2D.

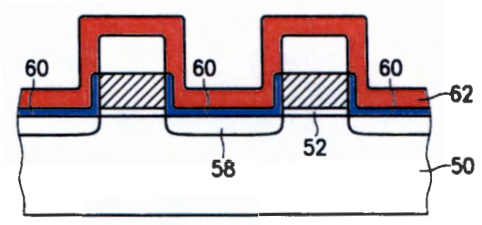


Fig. 2B

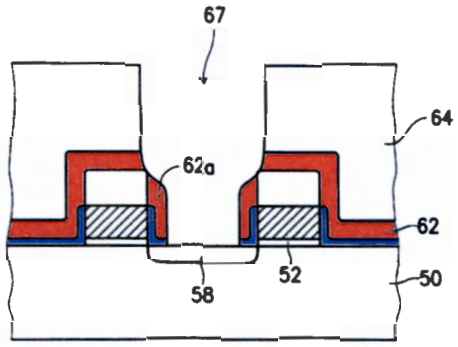


Fig. 2D

The specification makes clear that the claimed method eliminates one etch step and one deposition step from the prior art method. *Id.* at 3:5-9, 40-42. Defendants argue that Plaintiff's construction is improper because it would destroy that distinction. Defendants assert that the prior art method forms the spacers in two steps—(1) etching the first silicon nitride layer 22 to form spacers 22a, and (2) etching the second silicon nitride layer 24 to add "thickness" to those spacers. (D.I. 101 at 55). Therefore, Plaintiff's construction—"anisotropic etching of the silicon nitride layer also forms a spacer of silicon nitride"—includes the prior art method where two layers of silicon nitride are each etched to form part of the spacers. (*Id.* at 56).

Plaintiff argues that Defendants mischaracterize the prior art method. (*Id.* at 57-60). Plaintiff asserts that the second silicon nitride layer 24 does not form part of the spacer. The specification clearly describes the spacers 22a as being formed by etching the first silicon nitride layer 22. '997 patent at 1:35-37, Fig. 1C. Although Figure 1E shows that some portion of the second silicon nitride layer 24 remains on top of the spacers 22a, the specification does not identify any portion of layer 24 as part of the spacers.

I do not think the parties have a real claim construction dispute. The parties agree that the main thrust of the "simultaneously" limitation is to require the spacers to be formed in the same process step as the anisotropic etching of the silicon nitride layer. I do not think

Defendants' proposed negative limitation is necessary or helpful. It seems directed at a hypothetical infringement argument that Plaintiff has not raised. In fact, Plaintiff asserts that the argument is rooted in a misunderstanding of the prior art. (*See* D.I. 101 at 60 ("[T]he background art in the '997 [patent] does not show a spacer formed by two layers of nitride. This made-up feature is not what the '997 [patent] invention overcame and has nothing to do with the 'simultaneously' element.")). However, I agree that Plaintiff's proposed construction is somewhat ambiguous. Therefore, I adopt Plaintiff's proposed construction, but with the addition of the phrase "in the same process step" for clarity.

2. "diffusion region"; "providing a semiconductor substrate having a gate electrode and a diffusion region thereon" (claims 2 and 9)

a. Plaintiff's Proposed Construction: "area of substrate next to the gate electrode for the source/drain"; "providing a semiconductor substrate with a gate electrode and diffusion region"

b. Defendants' Proposed Construction: "source/drain"; "providing a semiconductor substrate on which the gate electrode and diffusion region have been formed"

c. Court's Construction: "area of substrate next to the gate electrode for the source/drain"; "providing a semiconductor substrate with a gate electrode and diffusion region"

Although both parties focus on the source/drain,[14] there is no real dispute that the "diffusion region" may include other features. (D.I. 101 at 64; D.I. 152 at 117:2-8, 120:8-13). The key issue for claim construction is whether the source/drain has been formed in the "diffusion region" at the start of the claimed method. (D.I. 152 at 120:8-15 (Defendants' counsel only disagreeing with Plaintiff's proposed construction based on the use of "for the" source/drain, as opposed to "having the" source/drain or "with the" source/drain)). The same analysis applies to both the term "diffusion region" and the related "providing" limitation.

[14] The source/drain is part of a transistor. (D.I. 101 at 64 n.30).

Defendants argue that a person of ordinary skill in the art would understand the source/drain to have already been formed at the start of the claimed method. (*Id.* at 69). The specification describes the preferred embodiment as starting with "source/drain diffusion regions 58 . . . defined in a semiconductor substrate 50 using known processes." '997 patent at 2:48-51, Fig. 2A. Defendants assert that a person of ordinary skill in the art would understand "defined" to mean "formed." (D.I. 101 at 68). Various deposition and etching steps are then performed, "completing the contact hole." '997 patent at 3:24. "Thereafter, a conductive plug can be formed in the contact hole 67 to electrically connect to the diffusion region 58." *Id.* at 3:25-26, Fig. 2D. Defendants argue that a person of ordinary skill in the art would understand "electrically connect[ing]" to require physical contact with the source/drain. (D.I. 102, Ex. B15 ¶¶ 49, 65). Therefore, as the specification does not mention additional processing to complete the source/drain, it must have been formed before the claimed method began, when the "source/drain diffusion regions" were "defined."

Defendants also point to the PTAB's *inter partes review* decision invalidating all claims, which was later reversed with respect to claims 2 and 9-14. (D.I. 66 at 2). The PTAB described Figure 2B as showing "diffusion regions 58" that "have been formed on substrate 50." (D.I. 102, Ex. B11 at 3). The PTAB did not specifically address the source/drain.

I do not find Defendants' arguments persuasive. The '997 patent does not reference formation of the source/drain, either in the claims or the specification. Defendants rely heavily on their expert's interpretation of the specification's discussion of the preferred embodiment. However, the preferred embodiment is not necessarily limiting and extrinsic evidence is less reliable than the patent and its prosecution history. *Phillips*, 415 F.3d at 1318, 1323. The PTAB opinion is also unavailing. The PTAB merely stated in passing that the "diffusion regions" had

been formed and did not discuss the source/drain. Therefore, I reject Defendants' proposed construction.

Plaintiff's proposed construction is consistent with a plain reading of the patent. The claims merely require a "diffusion region" without further limitation. The specification associates the "diffusion region" with the source/drain, but never indicates that there is a temporal limitation on when the source/drain is formed. '997 patent at 2:48-50. Therefore, I adopt Plaintiff's proposed construction.

3. "etching an opening through the insulating layer self-aligned and borderless" (claims 2 and 9)

a. Plaintiff's Proposed Construction: "etching an opening through the insulating layer that can be partially aligned by structure(s) other than the mask"

b. Defendants' Proposed Construction: "etching an opening through the insulating layer that is aligned by structure(s) in addition to the mask and has no contact borders"[15]

c. Court's Construction: "etching an opening through the insulating layer that is aligned by structure(s) in addition to the mask and has no contact borders"

The parties essentially dispute the construction of two terms—"self-aligned" and "borderless."

"self-aligned"

The specification states, "Self-alignment is a technique in which multiple levels of regions on the [semiconductor] wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks." '997 patent at 1:11-14. The parties appear to agree that "self-aligned" is a term of art and that it generally means aligned by structures in addition to the mask. (D.I. 101 at 76; D.I. 152 at 138:14-15, 139:13-18). Plaintiff argues,

[15] Defendants proposed this modified construction at the Markman hearing.

however, that a juror could misunderstand the self-alignment process to require alignment by other structures *without* use of the mask. (D.I. 101 at 83). Therefore, Plaintiff proposes the construction, "etching an opening through the insulating layer that can be partially aligned by structure(s) other than the mask."

The phrase "partially aligned" is nebulous and does not appear to be a term of art. (*Id.* at 79). Thus, Plaintiff's proposed construction seems likely to promote, rather than curb, jury confusion. I do not think there is any real dispute that Defendants' proposed construction is technically correct, as it is consistent with the definition provided by Plaintiff's expert. (D.I. 101 at 76). Thus, I adopt Defendants' proposed construction for "self-aligned" as meaning "aligned by structure(s) in addition to the mask."

"borderless"

As part of its background description of self-alignment, the specification states, "[T]he mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed." '997 patent at 1:18-20. Plaintiff argues that there is a difference between a process where "no contact borders are needed" and an opening where no borders exist. (D.I. 101 at 81; *see also* D.I. 152 at 147:12-16 (Plaintiff's counsel stating "it's possible" for a borderless process to have borders)).

The claims explicitly require "etching an opening through the insulating layer self-aligned and borderless." *E.g.*, *id.* at 4:41-42. Defendants propose that "borderless" means having no contact borders. (D.I. 152 at 138:15-16). Defendants' proposed construction is consistent with the plain and ordinary meaning of "borderless." Plaintiff has failed to justify departing from that plain and ordinary meaning to include an opening with borders. Therefore, I adopt Defendants' proposed construction for "borderless" as meaning "has no contact borders."

The parties should provide a proposed order construing the terms suitable for submission to a jury.

IT IS SO ORDERED this 21 day of August 2019.

United States District Judge