THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., Defendants.	: : : : : : : : :	C.A. No. 14-1430-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. MICRON TECHNOLOGY, INC., et al. Defendants.	: : : : : : : : :	C.A. No. 14-1431-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. SK HYNIX INC., et al. Defendants.	: : : : : : : : :	C.A. No. 14-1432-LPS-CJB

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MEMORANDUM OPINION

April 13, 2020
Wilmington, Delaware

STARK, U.S. District Judge:

Elm 3DS Innovations, LLC ("Elm" or "Plaintiff") filed suit against Defendants Samsung Electronics Co., LTD., Samsung Semiconductor, Inc., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively, "Samsung"); Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Consumer Products Group, Inc. (collectively, "Micron"); and SK Hynix Inc., SK Hynix America Inc., Hynix Semiconductor Manufacturing America Inc., and SK Hynix Memory Solutions Inc. (collectively, "SK Hynix" and, together with Samsung and Micron, "Defendants") on November 21, 2014, alleging infringement of 13 patents, specifically U.S. Patent Nos. 7,193,239 (the "'239 patent"), 7,474,004 (the "'004 patent"), 7,504,732 (the "'732 patent"), 8,035,233 (the "'233 patent"), 8,410,617 (the "'617 patent"), 8,629,542 (the "'542 patent"), 8,653,672 (the "'672 patent"), 8,791,581 (the "'581 patent"), 8,796,862 (the "'862 patent"), 8,841,778 ("the '778 patent"), 8,907,499 (the "'499 patent"), 8,928,119 (the "'119 patent"), and 8,933,570 (the "'570 patent") (collectively, the "patents-in-suit"). (D.I. 1)[1] The patents-in-suit generally relate to semiconductor technologies in the design and manufacture of three-dimensional integrated circuits. The parties submitted their joint claim construction brief on November 13, 2019. (D.I. 236) The Court held a claim construction hearing on January 9, 2020. (D.I. 243 ("Tr."))

I. LEGAL STANDARDS

A. CLAIM CONSTRUCTION

The proper construction of a patent is a question of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 837 (2015) (citing *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 388-91 (1996)). "It is a bedrock principle of patent law that the claims of a patent

[1] Unless otherwise noted, all references to the docket index are to C.A. No. 14-1430-LPS.

define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal quotation marks omitted).

"[T]here is no magic formula or catechism for conducting claim construction." *Id.* at 1324. Instead, the Court is free to attach the appropriate weight to appropriate sources "in light of the statutes and policies that inform patent law." *Id.*

"[T]he words of a claim are generally given their ordinary and customary meaning . . . [which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13 (internal citations and quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). The patent specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

While "the claims themselves provide substantial guidance as to the meaning of particular claim terms," the context of the surrounding words of the claim also must be considered. *Phillips*, 415 F.3d at 1314. Furthermore, "[o]ther claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment . . . [b]ecause claim terms are normally used consistently throughout the patent." *Id.* (internal citation omitted).

It is likewise true that "[d]ifferences among claims can also be a useful guide . . . For example, the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." *Id.* at 1314-15 (internal citation omitted). This "presumption is especially strong when the limitation in dispute is the only meaningful difference between an independent and dependent claim, and one

party is urging that the limitation in the dependent claim should be read into the independent claim." *SunRace Roots Enter. Co., Ltd. v. SRAM Corp.*, 336 F.3d 1298, 1303 (Fed. Cir. 2003).

It is also possible that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316. It bears emphasis that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." *Hill–Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014) (quoting *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)) (internal quotation marks omitted).

In addition to the specification, a court "should also consider the patent's prosecution history, if it is in evidence." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). The prosecution history, which is "intrinsic evidence," "consists of the complete record of the proceedings before the PTO [Patent and Trademark Office] and includes the prior art cited during the examination of the patent." *Phillips*, 415 F.3d at 1317. "[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

In some cases, "the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva*, 135 S. Ct. at 841. Extrinsic evidence "consists of all evidence external to the patent and prosecution history,

including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. For instance, technical dictionaries can assist the court in determining the meaning of a term to those of skill in the relevant art because such dictionaries "endeavor to collect the accepted meanings of terms used in various fields of science and technology." *Phillips*, 415 F.3d at 1318. In addition, expert testimony can be useful "to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id.* Nonetheless, courts must not lose sight of the fact that "expert reports and testimony [are] generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence." *Id.* Furthermore, "statements made by a patent owner during an IPR [inter partes review] proceeding . . . can be considered for claim construction." *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1362 (Fed. Cir. 2017). Overall, while extrinsic evidence "may be useful" to the court, it is "less reliable" than intrinsic evidence, and its consideration "is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." *Id.* at 1318-19. Where the intrinsic record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1308 (Fed. Cir. 1999) (citing *Vitronics*, 90 F.3d at 1583).

Finally, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007)

(quoting *Modine Mfg. Co. v. U.S. Int'l Trade Comm'n*, 75 F.3d 1545, 1550 (Fed. Cir. 1996)).

B. INDEFINITENESS

A patent claim is indefinite if, "viewed in light of the specification and prosecution history, [it fails to] inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). A claim may be indefinite if the patent does not convey with reasonable certainty how to measure a claimed feature. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1341 (Fed. Cir. 2015). But "[i]f such an understanding of how to measure the claimed [feature] was within the scope of knowledge possessed by one of ordinary skill in the art, there is no requirement for the specification to identify a particular measurement technique." *Ethicon Endo-Surgery, Inc. v. Covidien, Inc.*, 796 F.3d 1312, 1319 (Fed. Cir. 2015). A party seeking to prove indefiniteness must do so by clear and convincing evidence. *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017).

II. CONSTRUCTION OF DISPUTED TERMS

A. The "Substantially Flexible" Terms — Terms 1, 2, and 3[2]

Term 1[3] "substantially flexible substrate" "substantially flexible . . . substrate" "substrate is substantially flexible" "substrate substantially flexible" "substrate . . . is . . . substantially flexible" "substantially flexible . . . semiconductor layer"
Plaintiff Not indefinite. Plain and ordinary meaning, which is "a substrate/semiconductor layer that is largely able to bend without breaking"
Defendants Indefinite Alternatively, "substrate / semiconductor layer that has been thinned to a thickness of less than 50 microns and subsequently polished or smoothed"
Court Not indefinite. "A semiconductor substrate/semiconductor layer that is thinned to 50 μm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 2[4] "dice is substantially flexible" "die is substantially flexible"
Plaintiff Not indefinite. Plain and ordinary meaning, which is "dice/die that is largely able to bend without breaking"

[2] Term numbers correspond to the parties' Joint Claim Construction Chart. (*See* D.I. 194 App. A & B)

[3] These terms appear in claims 1 and 13 of the '239 patent; claims 36 and 51 of the '617 patent; claims 1, 40, and 44 of the '542 patent; claims 17, 84, 129, 143 of the '672 patent; claims 36, 54, 78, 116, and 136 of the '581 patent; claims 30, 34, 36, 135-37, and 147 of the '862 patent; claims 2, 8, 31, 44, 52, and 53 of the '778 patent; claims 1, 24, 53, 83, and 132 of the '499 patent; claims 1, 7, and 17 of the '119 patent; and claims 58 and 67 of the '570 patent.

[4] These terms appear in claims 60 and 70 of the '239 patent.

Defendants Indefinite Alternatively, "diced substantially flexible integrated circuit" (see construction of "substantially flexible integrated circuit")
Court Not indefinite. "A dice/die that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 3[5] "substantially flexible integrated circuit[s]" "substantially flexible integrated circuit layer[s]" "integrated circuits is substantially flexible" "integrated circuit . . . is . . . substantially flexible" "substantially flexible circuit layer[s]" "substantially flexible stacked integrated circuit structure" "substantially flexible circuit" "substantially flexible . . . structure"
Plaintiff Not indefinite. Plain and ordinary meaning, which is "an integrated circuit/integrated circuit layer/circuit layer/circuit structure/circuit/structure that is largely able to bend without breaking"
Defendants "[Integrated circuit[s] /integrated circuit layer[s] /stacked integrated circuit structure / structure] that contains a substantially flexible substrate where the dielectric material used in processing the substrate has a stress of 5×10^8 dynes/cm^2 tensile or less"
Court Not indefinite. "An integrated circuit/integrated circuit layer/circuit layer/circuit structure/circuit/structure that is largely able to bend without breaking and contains a substantially flexible semiconductor substrate, that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking, and a sufficiently low tensile stress dielectric material"

Certain Defendants – Samsung Electronics Co., Ltd., Micron Technology, Inc., and SK Hynix Inc. (collectively, "Petitioners") – instituted an *inter partes* review ("IPR") before the Patent Trial and Appeal Board ("PTAB") challenging the validity of patent claims that are

[5] These terms appear in claims 1, 22, 23, of the '004 patent; claims 1, 13, and 14 of the '732 patent; claims 1 and 40 of the '542 patent; claims 30, 135, and 147 of the '862 patent; claims 8, 44, and 46 of the '778 patent; claims 1, 12, 13, 24, 36-38, 49, 53, 83, 86, 87, and 132 of the '499 patent; claims 1 and 33 of the '119 patent; and claim 58 of the '570 patent.

asserted here.[6] The PTAB found that Petitioners had not met their burden to prove that the challenged claims were unpatentable, and the Federal Circuit subsequently affirmed these conclusions. *See generally Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1376 (Fed. Cir. 2019). In doing so, the Federal Circuit construed the "substantially flexible" terms, constructions which this Court now adopts as well. *See id.* at 1380.[7]

In pertinent part, the Federal Circuit stated as follows:

> Based on expert testimony from Dr. Franzon, the Board found that 'there are a number of factors that, within the context of semiconductor processing, determine the flexibility of a semiconductor substrate,' including the type of semiconductor substrate, the crystal orientation of the material, and the physical dimensions of the substrate. . . . This suggests thinning the semiconductor substrate to 50 μm and subsequently polishing or smoothing it is necessary but not necessarily sufficient to make the substrate substantially flexible. To ensure that the construction of 'substantially flexible' ***cannot be read to cover a rigid substrate or circuit layer***, we interpret a substantially flexible semiconductor substrate as a semiconductor substrate that is thinned to 50 μm and subsequently polished or smoothed such that it is largely able to

[6] The Petitions challenged the following: claims 17-18, 22, 84, 95, 129-32, 145-46, and 152 of the '672 patent (IPR2016-00386); claims 1-2, 8, 14, 31-32, 44, 46, and 52-54 of the '778 patent (IPR2016-00387); claims 10-12, 18-20, 60-63, 67, 70-73, and 77 of the '239 patent (IPR2016-00388 and IPR2016-00393); claims 1-3, 30-31, 33, 40-41, and 44 of the '542 patent (IPR2016-00390); claims 30, 34, 36, 135-38, and 147 of the '862 patent (IPR2016-00391); claims 36 and 51 of the '617 patent (IPR2016-00394); claims 1, 10-11, and 13-14 of the '732 patent (IPR2016-00395); claims 1, 7, 17-18, and 33 of the '119 patent (IPR2016-00687); claims 1 and 20-23 of the '004 patent (IPR2016-00691); claims 1, 12-13, 24, 36-38, 53, 83, 86-87, and 132 of the '499 patent (IPR2016-00708 and IPR2016-00770); and claims 58, 60-61, and 67 of the '570 patent (IPR2016-00786). *See generally Samsung*, 925 F.3d at 1376.

[7] The PTAB and Federal Circuit construed claim terms according to their "broadest reasonable interpretation in light of the specification." *Samsung*, 925 F.3d at 1376 n.4. The Court is not required to adopt the PTAB's or Federal Circuit's construction. *See SkyHawke Techs., LLC v. Deca Int'l Corp.*, 828 F.3d 1373, 1376 (Fed. Cir. 2016) ("Because the Board applies the broadest reasonable construction of the claims while the district courts apply a different standard of claim construction as explored in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), the issue of claim construction under *Phillips* to be determined by the district court has not been actually litigated.").

> bend without breaking. Likewise, we interpret a substantially flexible circuit layer as a circuit layer that is largely able to bend without breaking and contains a substantially flexible semiconductor substrate and a sufficiently low tensile stress dielectric material.

Samsung, 925 F.3d at 1380 (emphasis added).

The Federal Circuit's construction sets out three requirements, relating to (1) the substrate's thickness; (2) the substrate's processing; and (3) the substrate's flexibility. Specifically, the proper construction requires that the substrate "***is thinned to 50 µm* [*or less*] *and subsequently polished or smoothed such that it is largely able to bend without breaking***." *Id.* at 1379-80 (emphasis added).[8] Likewise, for the "circuit layer" and "integrated circuit" terms, the Federal Circuit "interpret[ed] a substantially flexible circuit layer as a circuit layer that is ***largely able to bend without breaking and contains a substantially flexible semiconductor substrate and a sufficiently low tensile stress dielectric material.***" *Id.* at 1380 (emphasis added).

Plaintiff urges the Court to construe the "substantially flexible terms" largely consistently with the Federal Circuit's construction, except to the extent that the Federal Circuit's

[8] The claims of the asserted patents describe how thinning and polishing a substrate is one way to form a substantially flexible substrate. For example, claim 31 of the '778 patent recites "the semiconductor substrate is thinned and polished or smoothed such that the semiconductor substrate is substantially flexible." *See also* '862 patent, claim 147 (reciting "the polished or smoothed backside [of a thinned, monocrystalline semiconductor substrate] enables the TTT substrate to be substantially flexible, and the polished or smoothed backside reduces the vulnerability of the TTT substrate to fracture as a result of flexing"). The specifications provide additional context. They note that the purpose of the invention is to provide a method of thinning and stacking substrates during semiconductor manufacturing. '672 patent at 8:64-10:26 ("Method A, 3Ds Memory Device Fabrication Sequence"); *see also id.* at 2:66-67, 3:5-8 (stating that feature of stacked circuit assembly technology includes "thinning of the memory circuit to less than about 50 µm in thickness forming a substantially flexible substrate"). Moreover, the specification of the '672 patent distinguishes "rigid" versus "substantially flexible" substrates. *E.g.*, '672 patent at 7:16-23.

construction limits the dielectric to low tensile stress. Plaintiff argues that the specification and claims do not limit the relevant stress value to tensile stress. (*See* D.I. 236 at 10 n.5) Plaintiffs offer no persuasive reason to depart from the Federal Circuit's understanding that the claims are limited to low tensile stress. Instead, the Court agrees with the Federal Circuit that a prosecution history disclaimer here requires that a substantially flexible circuit layer must contain low tensile stress dielectric material. *See Samsung*, 925 F.3d at 1379 ("Considered in its entirety, the prosecution history clearly and unambiguously demonstrates that a substantially flexible circuit layer, and similar terms, ***must contain a substantially flexible semiconductor substrate and a sufficiently low tensile stress dielectric material.***") (emphasis added).

Defendants take the view that the Federal Circuit's construction renders the claims indefinite because whether the substrate is "largely" able to bend without breaking is subjective; to Defendants, there is no objective boundary for the degree of bending that distinguishes substrates "largely able to bend" from those that bend less "largely" before breaking. (D.I. 236 at 11-12) In Defendants' view, the Federal Circuit's construction adds a term of degree lacking any boundary in the intrinsic evidence. (*See id.* at 15-16) This is true, according to Defendants, even though the intrinsic evidence identifies many properties that may affect the degree and type of bending. (*See id.*) Plaintiff responds that the PTAB's and Federal Circuit's ability to construe these terms is evidence that they are not indefinite. (*See, e.g., id.* at 10)[9]

[9] Neither the PTAB nor the Federal Circuit expressly decided the question of indefiniteness, which is an issue outside the scope of IPR. *See, e.g., Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 2020 WL 543427, at *7 (Fed. Cir. Feb. 4, 2020) (holding that PTAB may not cancel claims for indefiniteness in IPR because, "although indefiniteness analysis involves general claim construction principles[,] . . . it does not follow that the Board may exceed its statutorily limited authority simply because an indefiniteness issue arises during claim construction. Instead . . . Congress viewed a challenge based on indefiniteness to be distinct from a challenged based on sections 102 and 103."). However, Defendants argued and briefed indefiniteness to both the PTAB and the Federal Circuit (*see* Tr. at 29-30) (defense counsel acknowledging) and

Defendants have not met their burden of proving, by clear and convincing evidence, that the "substantially flexible" terms are indefinite. Terms of degree, such as "substantially" and "largely," are not inherently indefinite.[10] *See Sonix Tech. Co., Ltd. v. Publications Intl., Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017) ("[W]e have held that the clause 'not interfering substantially' did not render a claim invalid as indefinite. . . . [W]e reasoned that the intrinsic evidence provided guidance as to the scope of the claims, including, inter alia, examples of noninterfering structures and criteria for their selection. . . . This guidance allowed a skilled artisan to compare a potentially infringing product 'with the examples in the specification to determine whether interference . . . is substantial.'"). Rather, when evaluating indefiniteness, the Court must determine whether the patent "provide[s] enough certainty to one of skill in the art when read in the context of the invention." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014) (holding terms of degree are not inherently indefinite as long as claim language provides enough certainty to one of skill in art when read in context of invention). To assess whether a term of degree is "reasonably certain," the Court must look at the term itself and any description or examples provided in the intrinsic record. *See Sonix Tech.*, 844 F.3d at 1377; *see also Exmark Mfg. Co. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F. 3d 1332, 1346-47 (Fed. Cir. 2018) (concluding that specification's description and annotated figures identifying invention's configuration provided reasonable certainty as to meaning of disputed term).

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there is nothing in the record to support a view that either the PTAB or Federal Circuit believed the claims before them were indefinite or that the constructions they adopted would render any claim indefinite.

[10] Moreover, "[e]xpressions such as 'substantially' are used in patent documents when warranted by the nature of the invention, in order to accommodate the minor variations that may be appropriate to secure the invention." *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1120 (Fed. Cir. 2002).

Although the Federal Circuit's construction involves a degree of approximation, Defendants have not shown that this would cause a person of ordinary skill in the art to lack reasonable certainty as to the scope of the "substantially flexible" claims.

The prosecution history provides additional clarity regarding claim scope. As the patentee explained during prosecution, the invention is an improvement over prior art substrates with high-stress dielectrics that could not be thinned and stacked to the point of being flexible, without significantly damaging the integrated circuit. (*See* D.I. 236 at 22) (citing D.I. 194 Ex. 15-48 at 2-3) ("[T]he [prior art reference] prevented integrated circuits from being thinned to the point of being flexible without the stress of the dielectric materials causing the integrated circuit to fracture and disintegrate.") The Federal Circuit found that the patentee disclaimed certain claim scope, writing: "[t]o overcome the examiner's objection, Elm clearly and unambiguously disclaimed claim scope. For a semiconductor substrate to be 'substantially flexible' according to the claims, it must be thinned to 50 microns or less and polished or smoothed." *Samsung*, 925 F.3d at 1379.

Additional guidance as to claim scope is found elsewhere in the Federal Circuit's opinion. The Court stated that the definition of "substantially flexible" applies to all of its uses: "a substantially flexible circuit layer, and similar terms, must contain a substantially flexible semiconductor substrate and a sufficiently low tensile stress dielectric material." *Id.* The Court further explained that "substantially flexible" is not so broad a term as to include rigid substrates and circuit layers. *Id.* at 1380.

Fundamentally, the Court is not persuaded, by clear and convincing evidence, that a person of ordinary skill in the art, in the context of the three-dimensional technology described in

the asserted patents, would be unable to discern with reasonable certainty the difference between a rigid substrate, a physically bent substrate, and a broken substrate.

B. "Stress of 5 x 10^8 dynes/cm^2" and the "Low Stress" Terms – Terms 4 and 5

Term 4[11] "have stress of about 5 × 10^8 dynes/cm^2 or less" "have a stress of about 5 × 10^8 dynes cm^2 or less" "having a stress of 5 x 10^8 dynes/cm^2 or less" "a stress of about 5 × 10^8 dynes/cm^2 or less" "having a stress of 5 × 10^8 dynes/cm^2 tensile or less" "[have] a stress of about 5 × 10^8 dynes/cm^2 tensile or less" "having[/has] a stress of less than 5 × 10^8 dynes/cm^2 tensile" "with a tensile stress of less than 5 × 10^8 dynes/cm^2" "with a stress of less than 5 × 10^8 dynes/cm^2 tensile" "has[/having] a tensile stress of less than 5 × 10^8 dynes/cm^2"
Plaintiff Not indefinite. Plain and ordinary meaning.
Defendants Indefinite. Alternatively, Micron and Samsung propose "having stress in the dielectric layer that is between 0 and 5 x 10^8 dynes/cm^2 in tensile"
Court Indefiniteness unable to be resolved at this stage of the case

[11] These terms appear in claims 11, 12, 19, 20, 62, 63, 72, and 73 of '239 patent; claim 20 of the '004 patent; claim 10 of the '732 patent; claim 36 of the '617 patent; claims 2, 3, 30, 31, 40, and 41 of the '542 patent; claims 17, 22, 84, 95, 129, 131, 145, 146, and 152 of the '672 patent; claims 12, 36, 54, 78, 116, and 136 of the '581 patent; claims 135-38 and 147 of the '862 patent; claims 1, 2, 8, and 14 of the '778 patent; claims 1, 12, 13, 24, 53, 83, 86, 87, and 132 of the '499 patent; claims 7 and 18 of the '119 patent; and claims 60 and 67 of the '570 patent.

Term 5[12] "low stress dielectric" "low stress dielectric layer" "low stress . . . dielectric material" "low-stress . . . dielectric material" "low-stress . . . dielectric layer" "low stress . . . dielectric layer"
Plaintiff Not indefinite. "A dielectric having a stress of less than 8×10^8 dynes/cm^{2}"
Defendants Indefinite Alternatively, Micron and Samsung propose "having stress in the dielectric layer that is between 0 and 5×10^8 dynes/cm^2 in tensile"
Court Indefiniteness unable to be resolved at this stage of the case

Defendants contend that the "stress" terms are indefinite. They assert that a person of ordinary skill in the art would not know what type of stress to measure, or how and when to measure that stress on a dielectric layer. (D.I. 236 at 32, 39-42) In the alternative, Defendants Micron and Samsung argue that Terms 4 and 5 both mean "having stress in the dielectric layer that is between 0 and 5×10^8 dynes/cm^2 in tensile." (D.I. 236 at 42-47)

Defendants have not proven by clear and convincing evidence that Terms 4 and 5, claiming "stress of 5×10^8 dynes/cm^2" and "low stress," are indefinite. However (and unlike for Terms 1, 2, and 3 discussed above), the Court cannot determine at this stage of the case whether Terms 4 and 5 render the claims invalid as indefinite. Defendants will have an opportunity to renew their indefiniteness argument at the summary judgment stage (and, if necessary, at trial).

A person of ordinary skill would understand, as the patents explain, that a primary concern in semiconductor manufacturing is preparing substrates that are planar or flat. *See*, *e.g.*,

[12] These terms appear in claims 10, 18, 61, and 71 of the '239 patent; claims 1 and 21-23 of the '004 patent; claims 1, 13, and 14 of the '732 patent; claim 95 of the '672 patent; and claims 30 and 34 of the '862 patent.

'672 patent at 1:25-41, 7:42-57. When dielectric layers are formed on top of a substrate, stress in the dielectric will cause the substrate to curve, making it "impossible to successfully planarize by chemical mechanical processing." (D.I. 240 Ex. A (Baker Decl.) at 16) The asserted patents address this problem.

For example, the patents describe "layer stress" – e.g., the stress at the time the substrate is thinned; that is, the stress placed on the underlying substrate. *See, e.g.*, '672 patent at 4:17-30 ("[E]ach memory array circuit layer is a thinned and substantially flexible circuit with net low stress"); '672 patent at 8:64-67 (assuming that "several circuit layers will be bonded to a common or support substrate and subsequently thinned," then stacked).

Both parties' experts describe the interaction between dielectric stress and the substrate. (*See* D.I. 240 Ex. A (Baker Decl.) at 12, 29-30 (discussing impact of dielectric stresses on thin substrates); D.I. 194 Ex. 14-15 (Franzon Decl.) at 19-31) The dielectric stress value is a singular number that is published and relied upon by chip designers to avoid fabrication problems from substrate warpage. (D.I. 240 Ex. A (Baker Decl.) at 10-16; D.I. 194 Ex. 14-15 (Franzon Decl.) at 19-20) Moreover, the formula for defining stress is undisputed, and both parties' experts have opined as to methods for identifying and determining stress of a dielectric, such as "measuring the average curvature of a wafer before and after the film deposition." (*E.g.*, D.I. 236 at 25) (citing Murray Decl. at ¶ 39) Thus, a person having ordinary skill in the art ("POSA") might understand the scope of the claimed numeric stress term "stress of 5×10^8 dynes/cm^2" by relying on the intrinsic evidence of the asserted patents.

Defendants highlight other types of stress described in the patents. *See, e.g.*, '239 patent at 9:12-16 (describing "intrinsically low stress deposited film"); '695 patent at 6:22-30 (describing "extrinsic net surface stress"); '695 patent at 6:22-30 (describing "acceptable surface

stress levels"). Plaintiff's expert, Dr. Baker, also describes additional types of stress, including "thermal stresses," "growth stresses," and "residual stress." (D.I. 240 Ex. A (Baker Decl.) at 12-13, 26, 28) Moreover, both parties' experts describe the many different measurement techniques that persons of skill in the art could use to measure stress, which may result in varying values of reported stress. (D.I. 240 Ex. A (Baker Decl.) at 20-21, 30; D.I. 239 Ex. C (Murray Decl.) at 15-19) The common specification of the asserted patents, however, never describes which method should be used to approximate stress in dielectric layers of materials. In addition, Defendants have presented evidence tending to show that, depending on where stress is measured, "different values would be obtained" for stress at different points in the layer. (D.I. 240 Ex. A (Baker Decl.) at 6, 8, 17-18, 29)

Plaintiff argues that these other types of stress described in the patents are not at issue; instead, the stress described in the claims of the asserted patents "is the stress that the dielectric layer imposes on the underlying substrate." (D.I. 236 at 49) (citing '672 patent at 4:17-30) This stress, Plaintiff argues, "is a material property of the dielectric itself, but it has a stress value." (Tr. at 53-54) Plaintiff further contends that the relevant stress is the "force per unit area that is acting on a surface of a solid" – e.g., the stress as a whole surface, and not at a particular point. (Tr. at 60-61) Plaintiff agrees that there are various methods to measure stress, including the "curvature method," but the patents do not require a specific method of measurement. (D.I. 236 at 50) (citing D.I. 239 Ex. C (Murray Decl.) at 16) Thus, Plaintiff agrees that these variables – e.g., type of stress, how to measure stress, and where stress is measured – are considered by a POSA.

Because the claims are limited to a particular type of stress, measured at a specific place and time, the proper construction for Term 4 is not "plain and ordinary" meaning. But the Court

is unable to determine, at this stage of the case, whether Defendants can meet their burden to prove, by clear and convincing evidence, that this term renders the claims indefinite.

Term 5 involves claim terms describing "low stress." Both parties' proposed constructions are examples of "low stress" dielectric values, but neither side provides a persuasive basis for limiting the claims to exemplary embodiments from the specification. For example, the specification and prosecution history of the asserted patents do not limit the dielectric to a particular range – such as 0 to 5 x 10^8 dynes/cm^2, as Defendants Micron and Samsung have proposed. The reference to tensile stress of 5 x 10^8 dynes/cm^2 in the specification is merely an example, in which the specification confirms that a dielectric with tensile stress of 5 x 10^8 dynes/cm^2 would be sufficient. *See Samsung*, 925 F.3d at 1379.

Moreover, Plaintiff's proposed construction of "low stress" as "a dielectric having a stress less than 8 x 10^8/cm^2" is not supported in the specification or prosecution history. This value is referenced in the U.S. Patent 5,354,695 ("the '695 patent"), which the patents-in-suit have incorporated by reference. *See, e.g.*, '672 patent at 8:48-53 (describing low-stress silicon dioxide and silicon nitride dielectrics). The '695 patent explains that "low stress is defined relative to the silicon dioxide and silicon nitride deposition made with Novellus equipment as being less than 8 x 10^8 dynes/cm^2 in tension." '695 patent at 11:27-39. However, there is no evidence in the claims, specification, or prosecution history of the asserted patents that demonstrates an intent by the patentee to limit "low-stress" to an example described in a patent only incorporated by reference in the patents-in-suit.

To the extent the parties continue to have disputes relating to the meaning and/or indefiniteness of Terms 4 and/or 5, they shall raise those disputes again in the context of summary judgment motions.

C. The "Vertical Interconnection" Terms – Terms 6, 7, 8, and 9

Term 6[13] "vertically interconnected circuit block stacks" "vertically interconnected circuit blocks"
Plaintiff Plain and ordinary meaning, which is "vertically electrically connected circuit block stacks" and vertically electrically connected circuit blocks"
Defendants "[stacks of circuit layer blocks / blocks of circuit layers] electrically connected by conductors that pass vertically through at least one of the circuit layers"
Court "Vertically electrically connected circuit block stacks" and "vertically electrically connected circuit blocks"

Term 7[14] "a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits"
Plaintiff Plain and ordinary meaning of "vertical interconnect segments," which is "vertical electrical connections"
Defendants "Vertical interconnect segments" means "segments of electrical conductors that pass vertically through a circuit layer"
Court "Vertical electrical connections"

[13] These terms appear in claims 1, 5, 113, and 133 of the '581 patent, and claim 49 of the '499 patent.

[14] This term appears in claim 58 of the '570 patent.

Term 8[15] "Said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections"
Plaintiff Plain and ordinary meaning of "vertical interconnections," which is "vertical electrical connections"
Defendants "Vertical interconnections" means "electrical connections provided by conductors that pass vertically through a circuit layer"
Court "Vertical electrical connections"

Term 9[16] "At least one interconnection between two of the plurality of substrates"
Plaintiff Plain and ordinary meaning, which is "at least one electrical connection between two of the plurality of substrates"
Defendants "Interconnection between two of the plurality of substrates" means "electrical connection between two substrates provided by conductors that pass through one or more of the substrates"
Court "At least one electrical connection between two of the plurality of substrates"

The parties disagree over whether the term "vertical interconnection" requires a physical pass through the substrate – as opposed to connecting on the surface of the substrate – or along the outside surface of the stacked substrates. (*See* D.I. 236 at 54-60, 63-66, 68-69, 73-78) Defendants argue that the "interconnection" terms are practiced only by aspects of fine-grain interconnections that pass through a circuit layer. (*See* D.I. 236 at 68-73) Defendants contend that their proposed constructions provide clarity and specify which layers or substrates the interconnects pass through or connect. (D.I. 236 at 63-64)

[15] This term appears in claim 1 of the '004 patent.

[16] This term appears in claim 84 of the '672 patent.

The Court instead agrees with Plaintiff that the patents use the plain and ordinary meaning of "vertical interconnection" and do not require a pass through the substrate. Defendants' proposed construction improperly imports a limitation from the specification into the claims without evidence of the patentee's clear and unambiguous intent to limit claim scope. *See Liebel-Flarsheim*, 358 F.3d at 906. Defendants' proposed construction also problematically renders certain claims superfluous or redundant. *See generally Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so."). For example, claim 1 of the '119 patent requires both that the interconnections pass through the substrate and that there be "vertical interconnections." *See also* '617 patent at 13:19-21 (interconnection of "at least one conductive path that passes vertically through" substrate). Calling out in the claim that the interconnections must pass through the substrate would be unnecessary if Defendants were correct that the claimed "vertical interconnections" already require a pass through the substrate. If "vertical interconnections" imports the Defendants' limitation, this language would be unnecessary. Similarly, dependent claims that further require vertical interconnections to pass through the substrate would be rendered meaningless. *See, e.g.*, '542 patent claim 38 (describing vertical interconnect that "extends through one of a plurality of holes in semiconductor material"); '672 patent claim 14 ("conductive paths that pass through semiconductor material").

The specification defines vertical interconnections that pass through the substrate as "***fine-grain*** inter-layer vertical interconnects" (emphasis added). *E.g.*, '672 patent at 3:67-4:10 ("[T]he term fine-grain inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer without an intervening device element. . . . [T]he fine-grain inter-layer vertical interconnect also functions to bond together the various layers of the circuit."). But

where the patentee did not use the term "fine-grain inter-layer vertical interconnect," or refer to a specific embodiment, a POSA would not believe the patentee intended to limit vertical interconnections only to those that pass through the substrate.

The specification provides examples in which vertical interconnects do not always pass through the substrate. For example, the specification and claims of the '672 patent disclose conventional interconnections (which do not require passing through the substrate) to connect a logic or controller layer to a stack of 3D memory. *See* '672 patent at 3:1-2; *id.* at claim 35; *id.* at claim 39 (describing this concept, without requiring that interconnect pass through substrate); *see also* '672 patent at 4:31-48 (describing that if DRAM controller circuitry is part of larger die, then fine-grain vertical bus interconnect would be required to connect 3DS DRAM array circuit; otherwise, larger grain conventional interconnection could be incorporated into planarized bond layer). Other claims limit vertical interconnections between memory layers to embodiments that do not pass through the substrate, such as "wire bonding." *E.g.*, '004 patent at claim 19 ("wherein at least one of the interconnections is a wire bond," where referenced interconnections are vertical interconnections); *see also* '672 patent at 9:1-10:26 (describing Method A, with step that discusses use of conventional interconnections as part of iterative process where subsequent circuit layers are added to 3DS circuit stack before packaging).

Thus, unlike *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295 (Fed. Cir. 2004), which Defendants cite (*see* D.I. 236 at 71), here the Court finds distinctions in the patents' use of the term "vertical interconnect" that weigh against limiting the term in the manner proposed by Defendants. *Compare Irdeto*, 383 F.3d at 1301 ("[W]hile the specification does not contain any statements of explicit disavowal or words of manifest exclusion, it repeatedly,

consistently, and exclusively uses 'group' to denote fewer than all subscribers, manifesting the patentee's clear intent to so limit the term.").

Defendants quote from the "Summary of the Invention" and descriptions of preferred embodiments in the specification of the asserted patents to support their argument that the invention required the use of fine-grain vertical interconnections. (*See* D.I. 236 at 70-71) They further support this contention by citing to the patentee's criticism of the form of vertical interconnection in the prior art.[17] *See, e.g.*, '672 patent at 2:21-34. But "comparing and contrasting the present technique to that of the prior art does not 'rise to the level of [a] clear disavowal'" of claim scope. *Cont'l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 798 (Fed. Cir. 2019). Further, a patentee's reference to a single, preferred embodiment, does not require the Court to construe the claims as being limited to that embodiment. *See Info-Hold, Inc. v. Applied Media Techs. Corp.*, 783 F.3d 1262, 1267 (Fed. Cir. 2015). Thus, even if the inter-layer interconnections and conductive paths "pass through" the circuit layers in every embodiment of the asserted patents, as Defendants argue (*see* Tr. at 88), this does not amount to disavowal of claim scope. Nor does the Court find the required clear disavowal anywhere else in the intrinsic evidence.

[17] The patentee specifically criticized the prior art products for being too expensive for commercial use. *See* '672 patent at 2:21-34. The claimed 3D memory stack is less expensive due to several reasons, including, but not limited to, its vertical interconnection. *See* '672 patent at 1:41-58, 5:61-6:6, 6:66-7:15 (describing present invention's advantages over conventional monolithic circuits). While "fine grain vertical interconnections" can contribute to the improved performance over conventional memory devices (*see* '672 patent at 5:49-6:6), the patent does not require their use to achieve the invention's "objectives" – e.g., improved performance and lower manufacturing cost. (*See* D.I. 236 at 77; *see also* Tr. at 84 ("[T]here are other advantages that are a result of the invention, the ability to manufacture the memory layers separate from the logic layers, [and] a number of other ways to get advantages."))

D. The "Bond" and "Conductive Path" Terms – Terms 10, 11, 12, 13, 14, and 15

Term 10[18] "a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof " "a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"
Plaintiff Plain and ordinary meaning, which is "a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond forming material throughout a majority of the surface area thereof" "a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"
Defendants "a layer physically joining a majority of the surface area of first and second substantially planar surfaces of adjacent substrates to form interconnects between the two surfaces" "a layer, having a portion not at the edges of the adjacent dice, physically joining the substantially planar surfaces of adjacent dice to form interconnects between the two surfaces"
Court "a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond forming material throughout a majority of the surface area thereof" "a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"

Term 11[19] "Wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die"
Plaintiff "Wherein the semiconductor die is attached to the first surface of the substrate by one or more physical connections, including one physical connection located other than at the edges of the semiconductor die"

[18] These terms appear in claims 1 and 60 of the '239 patent.

[19] This term appears in claim 70 of the '239 patent.

Defendants "one location of the semiconductor die, other than at its edges, is physically joined to the first surface of the substrate to form interconnects therebetween"
Court "Wherein the semiconductor die is attached to the first surface of the substrate by one or more physical connections, including one physical connection located other than at the edges of the semiconductor die"

Term 12[20] "A first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate"
Plaintiff Plain and ordinary meaning of "the front surface or a back surface being bonded to the circuit substrate," which is "the front surface or a back surface being physically joined to the circuit substrate"
Defendants "The front surface or a back surface being bonded to the circuit substrate" means "the front surface or a back surface [of the first integrated circuit] is physically joined to the circuit substrate to form interconnects there between"
Court "The front surface or a back surface being bonded to the circuit substrate," which is "the front surface or a back surface being physically joined to the circuit substrate"

Term 13[21] "The first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" "Two of the plurality of substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal"
Plaintiff Plain and ordinary meaning, which is "physically joined in a fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal" "physically joined in fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal"

[20] This term appears in claim 1 of the '542 patent.

[21] These terms appear in claims 17 and 84 of the '672 patent.

Defendants "[the first and second substrates / two of the plurality of substrates] are physically joined in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon based dielectric material and metal to form interconnects therebetween" (*see* "predominantly" below)
Court "physically joined in a fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal" "physically joined in fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal"

Term 14[22] "A second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate" "a semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die"
Plaintiff Plain and ordinary meaning, which is "physically joined to the first surface of the first substrate to form electrically conductive paths between the first substrate and the second substrate" "physically joined to the first surface of the substrate with electrically conductive paths between the substrate and the die"
Defendants "[a second substrate / a semiconductor die having an integrated circuit formed thereon] physically joined to the first surface of the [first substrate / substrate] to form interconnects there between"
Court "physically joined to the first surface of the first substrate to form electrically conductive paths between the first substrate and the second substrate" "physically joined to the first surface of the substrate with electrically conductive paths between the substrate and the die"

[22] These terms appear in claims 13, 46, and 70 of the '239 patent.

Term 15[23] "Conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" "Conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate"
Plaintiff Plain and ordinary meaning, which is "electrically conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" "electrically conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate"
Defendants "Electrical connections formed by joining the first and second substrates so as to connect the interconnect contacts supported by the [topside / first] surface of the first substrate to the interconnect contacts supported by the second substrate"
Court "electrically conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" "electrically conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate"

Plaintiff proposes that the "bond" terms mean to physically join two materials. (D.I. 236 at 60) Defendants propose that the "bonding method must form a fine-grain inter-layer vertical interconnect to interconnect adjacent circuit layers or substrates in a 3DS memory device;" in other words, that bonding requires physically joining and forming a vertical interconnect at the same time. (D.I. 236 at 60, 66) The parties further disagree as to whether the "conductive path" terms describe conductive paths between stacked layers and formed through vertical interconnections. (D.I. 236 at 69) The Court agrees with Plaintiff on these disputes and adopts the plain and ordinary meaning for each of the "bond" and "conductive path" terms.

The patent claims explicitly indicate when the bonding method forms a fine-grain, inter-layer vertical interconnect. *See, e.g.*, '617 patent claim 1 ("a bond layer between the first surface

[23] These terms appear in claims 17, 129, and 143 of the '672 patent.

of the first substrate and the first surface of the second substrate, comprising, a plurality of bonds formed from the interconnect contacts of the first surfaces of the first and second substrate"). It follows that where the bonding method is not said to form a fine-grain, interlayer vertical connect, then the bonding method is not required to do so; it need merely physically join two materials.

Moreover, the specification describes the distinct processes of bonding and creating vertical interconnections. For example, the specification discusses the process by which a finished 3DS substrate is bonded to a conventional die or other substrate. *See* '672 patent at 10:6-26. In the "final bonding step," either "fine-grain interconnects" are formed between the 3DS memory circuit and the substrate or "conventional interconnect pattern[s]" can be formed after bonding. *Id.* It is not always required that fine-grain interconnects be formed.

The patents do not limit bond formation to a specific method. Instead, the '672 patent explains that "the invention contemplates bonding of separate memory controller and memory array substrates by any of various conventional surface bonding methods, such as anisotropically conductive epoxy adhesive, to form interconnects between the two to provide random access data storage." *See* '672 patent at 6:34-42. The specification expressly states that "the foregoing exemplary types of bond material choices should not be considered to be limitations on how the circuit layers can be bonded," including by use of conductive or nonconductive materials. *See* '672 patent at 8:8-19.

In context, then, Defendants' proposed constructions of the "bond" terms improperly seeks to import into the claims limitations from the specification embodiments. The Court is persuaded, instead, by Plaintiff and adopts the plain and ordinary meaning.

Similarly, the Court will adopt the plain and ordinary meaning of the disputed "conductive path" term. (D.I. 236 at 69) The intrinsic evidence does not support limiting "conductive path" to "electrical connections formed by joining" the stacked layers, as Defendants propose. (D.I. 236 at 69) (citing Fair Decl. (D.I. 210) at ¶¶ 160-61) Relying solely on expert testimony, Defendants argue that their proposed construction describes the only type of connection described or suggested by the specification. (*See id.*) However, as already noted, a specification's description of a preferred embodiment does not establish claim disavowal. *See Info-Hold, Inc.*, 783 F.3d at 1267.

E. "Thin" Terms – Term 16

Term 16[24] "Thin"
Plaintiff Not indefinite. No construction necessary.
Defendant Indefinite.
Court Not indefinite. No construction necessary.

The parties dispute whether the "thin" term is indefinite. (D.I. 236 at 78-83) Defendants argue that the term is an adjective that modifies portions of the claimed invention, such as the "structure," "layer," or "integrated circuit," without reference to the boundary between what constitutes "thin" and "not thin." (*Id.* at 82) Plaintiff contends that Defendants fail to show, with clear and convincing evidence, that the term is indefinite, pointing to numerous examples in the specification and claims that describe the terms "thinning," "thinned," or "thickness." *See, e.g.*,

[24] This term appears in claims 30, 135, and 147 of the '862 patent; claims 1, 12, 13, 24, 36, 37, 38, 49, 53, 83, 86, 87, and 132 of the '499 patent; and claim 58 of the '570 patent.

’672 patent at 4:17-30 (“[E]ach memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 µm and typically less than 10 µm in thickness.”).

Nominal circuit thickness is also described in the specification as 0.5 mm [500 microns] or greater. (*See id.*) The specification and prosecution history identify nominal thickness of a substrate that is “not thin” or outside the scope of the invention, and thin substrates, which range from 300-500 µm. (*See* D.I. 236 at 80-81) The Federal Circuit’s construction of “substantially flexible” requires the substrate to be thinned to 50 microns or less. *See Samsung*, 925 F.3d at 1380.

The Court agrees with Plaintiff that Defendants have failed to meet their burden to show that the “thin” terms are indefinite. The intrinsic evidence, as well as the Federal Circuit’s construction, strongly suggest to the Court that a POSA would understand, with reasonable certainty, how to distinguish “thin” from “not thin” in the context of the patents.

III. CONCLUSION

The Court will construe the disputed term as explained above. An appropriate Order follows.

THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ELM 3DS INNOVATIONS, LLC Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., Defendants.	: : : : : : : : :	C.A. No. 14-1430-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. MICRON TECHNOLOGY, INC., et al. Defendants.	: : : : : : : : :	C.A. No. 14-1431-LPS-CJB
ELM 3DS INNOVATIONS, LLC Plaintiff, v. SK HYNIX INC., et al. Defendants.	: : : : : : : : :	C.A. No. 14-1432-LPS-CJB

ORDER

At Wilmington this **13th** day of **April, 2020**:

For the reasons set forth in the Memorandum Opinion issued this date,

IT IS HEREBY ORDERED that the following claim terms of U.S. Patent Nos. 7,193,239; 7,474,004; 7,504,732; 8,035,233; 8,410,617; 8,629,542; 8,653,672; 8,791,581; 8,796,862; 8,841,778; 8,907,499; 8,928,119; and 8,933,570 are construed as follows:

Term 1	Court's Construction
"substantially flexible substrate" "substantially flexible . . . substrate" "substrate is substantially flexible" "substrate substantially flexible" "substrate . . . is . . . substantially flexible" "substantially flexible . . . semiconductor layer" ['239 patent claims 1, 13] ['617 patent claims 36, 51] ['542 patent claims 1, 40, 44] ['672 patent claims 17, 84, 129, 143] ['581 patent claims 36, 54, 78, 116, 136] ['862 patent claims 30, 34, 36, 135-37, 147] ['778 patent claims 2, 8, 31, 44, 52, 53] ['499 patent claims 1, 24, 53, 83, 132] ['119 patent claims 1, 7, 17] ['570 patent claims 58, 67]	Not indefinite. "A semiconductor substrate/semiconductor layer that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 2	Court's Construction
"dice is substantially flexible" "die is substantially flexible" ['239 patent claims 60, 70]	"A dice/die that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking"

Term 3	Court's Construction
"substantially flexible integrated circuit[s]" "substantially flexible integrated circuit layer[s]" "integrated circuits is substantially flexible" "integrated circuit . . . is . . . substantially flexible" "substantially flexible circuit layer[s]" "substantially flexible stacked integrated circuit structure" "substantially flexible circuit" "substantially flexible . . . structure" ['004 patent claims 1, 22, 23] ['732 patent claims 1, 13, 14] ['542 patent claims 1, 40]	Not indefinite. "An integrated circuit/integrated circuit layer/circuit layer/circuit structure/circuit/structure that is largely able to bend without breaking and contains a substantially flexible semiconductor substrate, that is thinned to 50 µm or less and subsequently polished or smoothed such that it is largely able to bend without breaking, and a sufficiently low tensile stress dielectric material."

['862 patent claims 30, 135, 147] ['778 patent claims 8, 44, 46] ['499 patent claims 1, 12, 13, 24, 36-38, 49, 53, 83, 86, 87, 132] ['119 patent claims 1, 33] ['570 patent claim 58]	

Term 4	**Court's Construction**
"have stress of about 5×10^8 dynes/cm^2 or less" "have a stress of about 5×10^8 dynes cm^2 or less" "having a stress of $5x10^8$ dynes/cm^2 or less" "a stress of about 5×10^8 dynes/cm^2 or less" "having a stress of 5×10^8 dynes/cm^2 tensile or less" "[have] a stress of about 5×10^8 dynes/cm^2 tensile or less" "having[/has] a stress of less than 5×10^8 dynes/cm^2 tensile" "with a tensile stress of less than 5×10^8 dynes/cm^2" "with a stress of less than 5×10^8 dynes/cm^2 tensile" "has[/having] a tensile stress of less than 5×10^8 dynes/cm^2" ['239 patent claims 11, 12, 19, 20, 62, 63, 72, 73] ['004 claim 20] ['542 patent claims 2, 41] ['732 patent claim 10] ['617 patent claim 36] ['672 patent claims 17, 22, 84, 129, 131, 145, 152] ['581 patent claims 12, 36, 54, 78, 116, 136] ['862 patent claims 135, 137, 138, 147] ['778 patent claims 1, 2, 8, 14] ['499 patent claims 1, 12, 13, 24, 53, 83, 86, 87, 132] ['119 patent claims 7, 18] ['570 patent claims 60, 67]	Indefiniteness unable to be resolved at this stage of the case

Term 5	**Court's Construction**
"low stress dielectric" "low stress dielectric layer" "low stress . . . dielectric material" "low-stress . . . dielectric material"	Indefiniteness unable to be resolved at this stage of the case

"low-stress . . . dielectric layer" "low stress . . . dielectric layer" ['239 patent, claims 10, 18, 61, 71] ['004 patent, claims 1, 21, 22, 23] ['732 patent, claims 1, 13, 14] ['672 patent, claim 95] ['862 patent, claims 30, 34]	

Term 6	Court's Construction
"vertically interconnected circuit block stacks" ['581, claims 1, 5, 113, 133] "vertically interconnected circuit blocks" ['499 patent claim 49]	"Vertically electrically connected circuit block stacks" and "vertically electrically connected circuit blocks"

Term 7	Court's Construction
"a plurality of vertical interconnect segments interconnecting the first and second integrated circuit layers, wherein each vertical interconnect segment forms an interconnection only between a pair of adjacent integrated circuits" ['570 patent claim 58]	"vertical electrical connections"

Term 8	Court's Construction
"Said plurality of first interconnection and said plurality of second interconnections are substantially aligned with each other, and said plurality of first interconnections and said plurality of second interconnections are electrically coupled together to form a plurality of vertical interconnections, including redundant vertical interconnections" ['004 patent claim 1]	"vertical electrical connections"

Term 9	Court's Construction
"At least one interconnection between two of the plurality of substrates" ['672 patent claim 84]	"at least one electrical connection between two of the plurality of substrates"

Claim Term 10	Court's Construction
"a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof " ['239 patent claim 1]	"a bonding layer physically joining together the adjacent substrates, the bonding layer being formed by physically joining first and second substantially planar surfaces having a bond forming material throughout a majority of the surface area thereof"
"a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice" ['239 patent claim 60]	"a bonding layer physically joining together the adjacent dice, the bonding layer physically joining first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice"

Claim Term 11	Court's Construction
"Wherein the semiconductor die is attached to the first surface of the substrate by one or more bonds including one bond located other than at the edges of the semiconductor die" ['239 patent claim 70]	"wherein the semiconductor die is attached to the first surface of the substrate by one or more physical connections, including one physical connection located other than at the edges of the semiconductor die"

Claim Term 12	Court's Construction
"A first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate." ['542 patent claim 1]	"the front surface or a back surface being physically joined to the circuit substrate"

Claim Term 13	Court's Construction
"the first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal"	"physically joined in a fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal"

['672 patent claim 17] "two of the plurality of substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon-based dielectric material and metal" ['672 patent claim 84]	 "physically joined in fixed relationship to one another at least mostly with metal, or at least mostly with silicon-based dielectric material and metal"

Claim Term 14	**Court's Construction**
"A second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate" ['239 patent claims 13, 46]	"physically joined to the first surface of the first substrate to form electrically conductive paths between the first substrate and the second substrate"
"A semiconductor die having an integrated circuit formed thereon bonded to the first surface of the substrate with conductive paths between the substrate and the die" ['239 patent claim 70]	"physically joined to the first surface of the substrate with electrically conductive paths between the substrate and the die"

Claim Term 15	**Court's Construction**
"Conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate" ['672 patent claim 17]	"electrically conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate"
"Conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate" ['672 patent claims 129, 143]	"electrically conductive paths between the interconnect contacts supported by the first surface of the first substrate and of the interconnect contacts supported by the second substrate"

Claim Term 16	**Court's Construction**

"Thin" ['862 patent claims 30, 135, 147] ['499 patent claims 1, 12, 13, 24, 36, 37, 38, 49, 53, 83, 86, 87, 132] ['570 patent claim 58]	Not indefinite. No construction necessary.

UNITED STATES DISTRICT JUDGE