IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INTEL CORPORATION,	:	
	:	
Plaintiff,	:	
	:	
v.	:	C.A. No. 14-377-LPS
	:	
FUTURE LINK SYSTEMS, LLC,	:	
	:	
Defendant.	:	

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MEMORANDUM OPINION

August 2, 2016
Wilmington, Delaware

STARK, U.S. District Judge:

On March 24, 2014, Plaintiff Intel Corporation ("Plaintiff" or "Intel") filed suit for declaratory judgment that patents owned by Defendant Future Link Systems, LLC ("Defendant" or "Future Link") are "not infringed, invalid, licensed, and/or exhausted." (D.I. 1 at 1-2) Intel's initial and first-amended complaints challenged nine patents: U.S. Patent Nos. 5,608,357 ("'357 patent"); 5,870,570 ("'570 patent"); 6,008,823 ("'823 patent"); 6,108,738 ("'738 patent"); 6,606,576 ("'6576 patent"); 6,622,108 ("'108 patent"); 6,636,166 ("'166 patent"); 6,920,576 ("'0576 patent"); and 7,478,302 ("'302 patent"). (D.I. 1 at 2; D.I. 95 at 1-2) On September 2, 2015, Future Link filed a Partial Answer and Counterclaims asserting eight additional patents against Intel: U.S. Patent Nos. 5,754,867 ("'867 patent"); 6,052,754 ("'754 patent"); 6,317,804 ("'804 patent"); 7,685,439 ("'439 patent"); 7,743,257 ("'257 patent"); 7,917,680 ("'680 patent"); 7,983,888 ("'888 patent"); and 8,099,614 ("'614 patent") (collectively with the nine patents originally challenged by Intel, "Patents-in-Suit"). (*See* D.I. 135 at 40) The Patents-in-Suit relate to a broad range of computer technology.[1]

Pending before the Court are claim construction disputes for thirteen claim terms across the following ten patents: the '357, '867, '570, '754, '804, '6576, '108, '302, '257, and '680 patents.[2] (D.I. 324 at 1) The parties submitted technology tutorials on April 28 (*see* D.I. 302, 304) and completed briefing on claim construction on May 12 (D.I. 288, 290, 315, 318). The

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[1]The Patents-in-Suit are attached as exhibits to Intel's First Amended Complaint (D.I. 95) and Future Link's Partial Answer and Counterclaims (D.I. 135).

[2]On May 27, the parties submitted a chart of all claims from the Patents-in-Suit that are either challenged by Intel (as not-infringed or invalid) and/or asserted by Future Link. (D.I. 341) The Court will only construe terms that are in claims identified by the parties in this chart.

Court held a claim construction hearing on June 6. (*See* Transcript, D.I. 351 ("Tr."))

I. LEGAL STANDARDS

The ultimate question of the proper construction of a patent is a question of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 837 (2015) (citing *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 388-91 (1996)). "It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal quotation marks omitted). "[T]here is no magic formula or catechism for conducting claim construction." *Id.* at 1324. Instead, the court is free to attach the appropriate weight to appropriate sources "in light of the statutes and policies that inform patent law." *Id.*

"[T]he words of a claim are generally given their ordinary and customary meaning . . . [which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13 (internal citations and quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). The patent specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

While "the claims themselves provide substantial guidance as to the meaning of particular claim terms," the context of the surrounding words of the claim also must be considered. *Phillips*, 415 F.3d at 1314. Furthermore, "[o]ther claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment . . . [b]ecause claim terms are

normally used consistently throughout the patent . . . ." *Id.* (internal citation omitted).

It is likewise true that "[d]ifferences among claims can also be a useful guide . . . . For example, the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." *Id.* at 1314-15 (internal citation omitted). This "presumption is especially strong when the limitation in dispute is the only meaningful difference between an independent and dependent claim, and one party is urging that the limitation in the dependent claim should be read into the independent claim." *SunRace Roots Enter. Co., Ltd. v. SRAM Corp.*, 336 F.3d 1298, 1303 (Fed. Cir. 2003).

It is also possible that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Phillips*, 415 F.3d at 1316. It bears emphasis that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014) (quoting *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)) (internal quotation marks omitted).

In addition to the specification, a court "should also consider the patent's prosecution history, if it is in evidence." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir 1995), *aff'd*, 517 U.S. 370 (1996). The prosecution history, which is "intrinsic evidence," "consists of the complete record of the proceedings before the PTO [Patent and Trademark Office] and includes the prior art cited during the examination of the patent." *Phillips*, 415 F.3d at 1317. "[T]he prosecution history can often inform the meaning of the claim language by

demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

In some cases, "the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva*, 135 S. Ct. at 841. Extrinsic evidence "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. For instance, technical dictionaries can assist the court in determining the meaning of a term to those of skill in the relevant art because such dictionaries "endeavor to collect the accepted meanings of terms used in various fields of science and technology." *Phillips*, 415 F.3d at 1318. In addition, expert testimony can be useful "to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id.* Nonetheless, courts must not lose sight of the fact that "expert reports and testimony [are] generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence." *Id.* Overall, while extrinsic evidence "may be useful" to the court, it is "less reliable" than intrinsic evidence, and its consideration "is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." *Id.* at 1318-19. Where the intrinsic record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper. *See Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1308 (Fed. Cir. 1999) (citing *Vitronics*, 90

F.3d at 1583).

Finally, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (quoting *Modine Mfg. Co. v. U.S. Int'l Trade Comm'n*, 75 F.3d 1545, 1550 (Fed. Cir. 1996)).

II. CONSTRUCTION OF DISPUTED TERMS[3]

A. '357 Patent

"buffer memory . . . for removing jitter"[4]

Future Link "buffer memory . . . for removing the offset of data transition locations from their ideally clocked positions"
Intel "buffer memory . . . for the intended purpose of eliminating dynamic or short-term skews from an ideal signal"
Court "buffer memory . . . for removing the offset of data transition locations from their ideally clocked positions"

The parties have several disputes related to this claim term. First, the parties dispute whether the word "removing" should be given its plain and ordinary meaning or whether it should be construed as "eliminating" ***all*** jitter. The Court agrees with Future Link that the word "removing" does not require elimination of all jitter. The plain and ordinary meaning of

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[3]The parties have agreed to certain constructions, all of which the Court will adopt.

[4]This term appears in claims 1-27 of the '357 patent.

"removing" is not synonymous with "removing ***all***." Moreover, the specification of the '357 patent discloses embodiments of the invention that are ***not*** designed to remove ***all*** jitter. (*See* '357 patent at 10:38-41 ("[T]he FIFO device (or phase aligning system) may also include a bit slip detect circuit 962 which produces an error signal 964 ***when the amount of jitter is too much for the phase aligning system 300 to absorb***.") (emphasis added); *id.* at 5:3-4 (describing "phase aligning system 300" as embodiment of invention); *see also id.* at 8:53-54 ("[T]he jitter ***up to a predetermined amount*** is removed by the FIFO device 800.") (emphasis added); *id.* at 9:27-30 ("In this implementation, ***the maximum jitter amount that the FIFO device 800 can handle is four unit interval*** if data is arriving too fast and three unit intervals if the data is arriving too slow.") (emphasis added)) Because Intel's proposed construction reads in a limitation that is not required by the specification, and because the word "removing" is sufficiently understandable for a jury without further construction, the Court will construe the word "removing" to have its plain and ordinary meaning, as proposed by Future Link.

Next, the parties dispute the definition of "jitter." Future Link proposes a definition from a patent cited during prosecution of the '357 patent. (D.I. 288 at 2) (citing U.S. Patent No. 4,821,297 at 7:1-4 (defining jitter as "the offset of data transition locations from their ideally clocked positions")) Intel argues that the specification "explicitly defines 'jitter'" as "dynamic skews." (D.I. 290 at 4) Intel also cites extrinsic dictionary definitions of "jitter" as "short-term skews." (*Id.*) The Court agrees with Future Link's definition of jitter. Rather than narrowly define "jitter," the entirety of the intrinsic record – including the cited-patent source of Future Link's definition of "jitter" – appears to characterize "jitter" as a broader term which encompasses, but is not limited to, the "dynamic skews" mentioned in the '357 patent.

Therefore, the Court will adopt Future Link's definition of "jitter."

Finally, the parties dispute whether the Court should construe this term to include an "intended purpose" for the "buffer memory" component referred to in the disputed term. The Court agrees with Future Link that the intrinsic record does not require an "intent" element to be added to the Court's construction. The Court agrees with Future Link that Intel's cited portions of the intrinsic record refer to an outcome that the buffer memory provides rather than an aspirational objective of the buffer memory component. (*See* D.I. 315 at 2) In addition, the Court agrees with Future Link that there is no disclaimer or disavowal in the specification or prosecution history that would require Intel's "intended purpose" limitation. (*See id.* at 3)

For the foregoing reasons, the Court will adopt Future Link's proposed construction for this term.

B. '867 Patent

"means for selecting an external to internal clock frequency ratio"[5]

Future Link Function: "selecting an external to internal clock frequency ratio" Structure: "a signal sent to a BUS FREQUENCY pin of the CPU"
Intel Function: "selecting an external to internal clock frequency ratio" Structure: "a signal sent to a RESET pin, a RESET pin, a signal sent to a BUS FREQUENCY pin, and a BUS FREQUENCY pin"

[5]This term appears in claims 1, 2, and 4 of the '867 patent.

Court
Function: "selecting an external to internal clock frequency ratio" Structure: "a signal sent to a RESET pin, a RESET pin, a signal sent to a BUS FREQUENCY pin, and a BUS FREQUENCY pin"

The parties agree that this term should be construed pursuant to 35 U.S.C. § 112, ¶ 6.[6] The parties also agree upon the function for this means-plus-function term. The parties disagree, however, about the corresponding structure. Intel argues that RESET and BUS FREQUENCY pins and corresponding signals are required to select an external to internal clock frequency ratio. Future Link argues that only a BUS FREQUENCY signal is required. The Court agrees with Intel's proposed construction.

The language of claim 1 makes clear that "altering said means for selecting an external to internal clock frequency ratio" is done "to lower the power consumption by said CPU and therefor power consumption of said computer system while maintaining maximum performance of said computer system." ('867 patent at 3:47-53) Therefore, according to the claim language, ***only*** the "means for selecting an external to internal clock frequency ratio" may accomplish these claimed objectives by being "alter[ed]." In addition, there is only one structure described in the specification that, when altered, will accomplish the claimed power consumption and performance characteristics – namely, the combination of RESET and BUS FREQUENCY pins with signals sent to these respective pins. (*See id.* at 3:10-20) The specification clearly ***requires*** use of the RESET pin to select a frequency ratio. (*See id.* at 3:17-20)

Future Link argues that the function associated with this term requires "selecting" and

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[6]The parties agree as to the applicability of 35 U.S.C. § 112, ¶ 6 for all of the disputed means-plus-function terms in the Patents-in-Suit.

attempts to distinguish "selecting" from actually "changing" the frequency ratio. (D.I. 288 at 6-8) However, as already discussed, the surrounding claim language indicates that the "means for selecting" must actually ***change*** the frequency ratio. "Proper claim construction . . . demands interpretation of the entire claim in context, not a single element in isolation." *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999). The Court rejects Future Link's attempt to distinguish "select" from "change."[7]

Future Link also argues that the doctrine of claim differentiation supports a presumption that the "power-on reset means for selecting an external to internal clock frequency ratio" recited in claim 5 is not present in claim 1 and, therefore, that the RESET pin and signal are not required elements of the structure recited in claim 1. (*See* D.I. 315 at 7) The Court agrees that the additional "***power-on***" limitation in claim 5 narrows claim 5's scope from what is claimed in claim 1. However, this narrowing does not necessarily mean that a RESET pin and signal are not included in claim 1. In fact, both claims require "reset" functionality, for the reasons described above. Claim 5 is nevertheless narrower because it requires a reset at "power-on" while claim 1 does not. "'It is not necessary that each claim read on every embodiment.'" *PPC Broadband, Inc. v. Corning Optical Commc'ns RF, LLC*, 815 F.3d 747, 755 (Fed. Cir. 2016) (quoting *Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010)).

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[7]Future Link draws attention to Intel's originally proposed construction for the structure associated with this term: "a RESET pin and a BUS FREQUENCY pin, ***which are a physical pin that resets the processor and a physical pin used to select the external to internal clock frequency ratio, respectively***." (D.I. 288 at 7) (emphasis in original) Future Link argues that this construction shows how Intel's "additional structure . . . performs a function different than the recited function of 'selecting,'" namely, "reset[ing]." (*Id.*) The Court declines to give dispositive weight to a construction that was later abandoned by Intel. In addition, as already explained, the "selecting" and "changing" here are accomplished by the same structure and describe the same functionality.

For the foregoing reasons, the Court will adopt Intel's proposed construction for this term.

C. '570 Patent

"identification device select decoder"[8]

Future Link "a decoder that identifies the target of a configuration access"
Intel "a decoder of an initialization device select (IDSEL) signal, as defined by the PCI Local Bus Specification"
Court "a PCI-compliant decoder that identifies the target of a configuration access"

Intel argues that this term should be limited to cover only a decoder of a specific signal used in the Peripheral Component Interconnect ("PCI") architecture. (*See* D.I. 290 at 9-12) Future Link argues for a broader construction that tracks language from the specification. (*See* D.I. 288 at 8-11) (citing '570 patent at 8:66-9:1) The Court will include the language from Future Link's proposed construction in the Court's construction, because it will aid the jury by describing the function of an "identification device select decoder" in the context of the patent. However, the Court will also include in its construction a requirement that the decoder must be PCI-compliant. The intrinsic record strongly supports the conclusion that the scope of the claims is limited to PCI-compliant embodiments and Future Link has identified no evidence to the contrary.

Future Link argues that this term should not be limited to covering only decoders of an initialization device select ("IDSEL") signal defined in PCI specifications. There is substantial

[8]This term appears in claims 1-14 and 17-18 of the '570 patent.

intrinsic evidentiary support for Future Link's position. For example, claim 17 includes the term "identification device select decoder" without referring to PCI. In this regard, claim 17 stands in contrast to all of the other claims in the '570 patent, each of which explicitly refer to PCI. The prosecution history reveals that this distinction between claim 17 and the other claims was purposeful, in that the applicants purposely attempted to remove "the limitation of PCI compliance" from claim 17 during prosecution. (D.I. 276-7 Ex. NN at 6-7) Claim 18, which depends from claim 17 and was added concurrently with claim 17, adds a limitation that the "bus agents" referenced in claim 17 must be PCI-compliant, invoking a claim-differentiation presumption that at least the bus agents in claim 17 need ***not*** be PCI-compliant. In light of the above, the Court rejects Intel's construction as overly narrow, because the prosecution history clearly evinces the applicants' intent to broaden claim 17, and because there is no disclaimer or disavowal in the intrinsic evidence that would require this term to be limited to any specific version of the PCI specifications or to the IDSEL signal described therein.

However, the Court agrees with Intel that this claim term should be limited to PCI bus architectures. The specification of the '570 patent makes it clear that the invention is limited to implementations on PCI bus architectures. (*See, e.g.*, '570 patent at 4:17-18) ("The system of the present invention provides sufficient resources to ensure PCI bus protocols are complied with.") Plaintiff acknowledges that all of the embodiments disclosed in the specification include PCI. (*See* Tr. at 67) The entirety of the "Disclosure of the Invention" section of the patent exclusively refers to PCI functionality. (*See id.* at 3:48-4:27) Every embodiment disclosed in the detailed description of the invention uses PCI. (*See generally id.* at 4:57-10:50; *see also MySpace, Inc. v. GraphOn Corp.*, 672 F.3d 1250, 1256 (Fed. Cir. 2012) ("An inventor is entitled to claim in a

patent what he has invented, but no more."))

Intel's arguments regarding the prosecution history of the '570 patent are also persuasive. Intel points out that, although the ***bus agents*** recited in claim 17 do not need to be PCI-compliant after addition of claims 17 and 18 during prosecution, the "multiple bus agent integrated circuit device" claimed in claim 17 still includes an "identification device select decoder" which is defined in relation to PCI specifications. (D.I. 290 at 12) In fact, the only "identification device select decoder" referred to in the specification is PCI-compliant. (*See* '570 patent at 4:46-48 (referring to Figure 6 as depiction of "identification device select decoder"); *id.* at 8:42-9:36 (describing identification device select decoder in Figure 6 as PCI-compliant)) Thus, claim 17's removal of all ***express*** references to "PCI" will not be construed as broadening the scope of the claims beyond the PCI-compliant device that the applicants described as their invention in the specification. *Honeywell*, 452 F.3d at 1319.

For the foregoing reasons, the Court will construe "identification device select decoder" as "a PCI-compliant decoder that identifies the target of a configuration access."

D. '754 Patent

"external bus control circuit"[9]

Future Link "circuitry which controls the shared signals of the circuit blocks, and which is external to the plurality of circuit blocks"
Intel "circuitry external to a circuit block that allows the circuit block to be connected to a wide variety of shared bus standards while the circuit block's internal circuitry remains unchanged"

[9]This term appears in claims 1-3, 5, 7-9, and 14 of the '754 patent.

Court "circuitry external to circuit blocks, wherein the circuitry is part of an apparatus for providing communication that allows a plurality of circuit blocks to be connected to a wide variety of shared bus standards while the circuit blocks' internal circuitry remains unchanged"

Intel argues that this term should be limited to implementing a key advantage of the invention: providing a system "which enables circuit components of a computer system to be connected in a wide variety of shared bus schemes while remaining substantially unchanged." ('754 patent at 2:23-26) The Court agrees that the claims must be limited to covering only apparatuses that implement this key advantage. The specification shows a clear intention to exclude implementations that do not include this key advantage by defining the invention as "provid[ing] this advantage" and by disparaging prior art implementations that do not include the advantage. (*See id.* at 2:5-34) The Court rejects Future Link's proposed construction because it does not include this limitation.

The parties' proposed constructions may imply that the "external bus control circuits" are the only components that control connection to a bus or busses in independent claims 1 and 9. The claim language indicates that "an external arbitration control unit" in claim 1 or "an external address arbitration control unit" in claim 9 are also involved in establishing communication pathways involving the bus or busses. The Court's construction includes the key advantage discussed above without implying that the external bus control circuits are the sole components controlling bus arbitration, which may otherwise be confusing to a jury. Independent claims 1 and 9 are each broadly directed to an "apparatus for providing communication," and it is the "apparatus" ***as a whole*** that must implement the key advantage rather than the external bus control circuits by themselves.

For the foregoing reasons, the Court will construe "external bus control circuit" to mean "circuitry external to circuit blocks, wherein the circuitry is part of an apparatus for providing communication that allows a plurality of circuit blocks to be connected to a wide variety of shared bus standards while the circuit blocks' internal circuitry remains unchanged."

"slave port"[10]

Future Link "a port which is capable of accepting a read and/or write cycle from another module"
Intel "interface circuitry directed by a master port and capable of transmitting and receiving information to and from the master port"
Court "a port which is capable of responding to a master port by transmitting information, receiving information, or both"

Intel proposes replacing the word "port" in this term with "interface circuitry" (D.I. 318 at 14), while Future Link disagrees (D.I. 288 at 14-15). The Court agrees with Future Link that inclusion of "interface circuitry" in the Court's construction for this term is unnecessary and could potentially confuse a jury.

Regarding the word "slave," the Court rejects both parties' proposed constructions. Future Link attempts to read in a limitation from the embodiment depicted in Figure 3 and described in accompanying text. (*See* D.I. 288 at 14) (citing '754 patent at 6:61-64) There is no clear intention in the specification to limit the claims to the embodiment shown in Figure 3. Therefore, the Court rejects Future Link's proposed construction.

Intel's proposed construction would require the slave port to be "directed by a master

[10]This term appears in claims 1-3, 5, 7-9, and 14 of the '754 patent.

port." The claims do not clearly require such direction. The Court agrees with Future Link's argument that "the remaining claim language [in independent claims 1 and 9] 'for responding to a master port in transmitting or receiving information' strongly implies that 'slave port' should not itself be defined according to its communication capabilities relative to a master port, as Intel suggests." (D.I. 288 at 15) The claims make clear that direction of the slave port is not entirely accomplished by the master port, as could be implied in Intel's construction. (*See, e.g.*, '754 patent, claim 1 at 24:49-53) (reciting "external arbitration control unit" that "establish[es] dedicated communication pathways" between master and slave ports)

The claim language requires that the slave port respond to a master port by "transmitting or receiving information." The Court agrees with Future Link that "transmitting or receiving" in the context of the specification ('754 patent at 6:61-64) can cover ports that are capable of performing one or both of these functions. Therefore, the Court will include a limitation to this effect.

For the foregoing reasons, the Court will construe "slave port" as "a port which is capable of responding to a master port by transmitting information, receiving information, or both."

E. '804 Patent

"serial port"[11]

Future Link "a port that transfers bits, characters, or data units sequentially"
Intel "a port that transfers data one bit at a time"

[11]This term appears in claims 1-5, 8, 9, 16-18, 21-24, 26-28, and 40 of the '804 patent.

Court "a port that transfers information sequentially"

Intel's proposed construction is contradicted by the intrinsic evidence. Although the specification does not explicitly define the term "serial port," Figure 1 shows five serial ports (labeled 40, 42, 44, 46, and 48) that each communicate over dedicated "data," "command," and "clock" lines. (*See* '804 patent at 5:29-43) For a "read request command," certain information is "supplied on the data line concurrently with the read request command on the command line." (*See id.* at 9:65-67) Thus, the specification contemplates transfer of information to "serial ports" on multiple lines concurrently instead of "one bit at a time" on a single line, as implied by Intel's proposed construction.

Future Link's proposed construction is better-aligned with the intrinsic evidence, and the Court bases its construction on the intrinsic evidence. Future Link's construction also aligns with the extrinsic evidence presented by Intel. (*See, e.g.*, D.I. 290 at 16 n.6) (Intel citing dictionary definitions) As persuasively summarized by Future Link, Intel's extrinsic evidence demonstrates that "the term 'serial'" means that information is "transferred sequentially" in "single or multi-bit" units. (*See* D.I. 315 at 16) Thus, the Court will construe this term according to Future Link's proposed construction, but with the word "information" used in place of "bits, characters, or data units," because the latter phrase is vague (at least with respect to "data units") and may confuse a jury.

For the foregoing reasons, the Court will construe "serial port" as "a port that transfers information sequentially."

F. '6576 Patent

"calibration path for data calibration"[12]

Future Link "a path for passing calibration data between at least two nodes"
Intel "a path between at least two nodes for passing calibration information that is distinct from the data paths"
Court "a path for passing calibration data between at least two nodes"

Intel argues that the "calibration path" in this term must be "distinct from the data paths." Intel's proposed construction could be read as excluding at least one embodiment disclosed in the specification. (*See* '6576 patent at 4:45-60) ("In one example embodiment, this additional calibration path is selectively assigned to act either as a calibration data path for passing calibration data or as one of the data paths for passing a respective one of the N bits of data in parallel. In one application, this selective assignment rotates through each of the M data paths while using the remaining M–1 data paths for passing . . . data unrelated to the calibration[].").

Intel argues that the prosecution history evidences a disavowal of calibration paths that are not distinct from data paths. (*See* D.I. 290 at 19) (noting examiner's rejection over prior art reference that described "transmitting 'a calibration signal . . . over [a] parallel communication bus' between two nodes" and quoting applicant's response to the rejection that the reference "'fail[ed] to teach a calibration path as claimed'") This purported disavowal is unclear at best. Because the specification contemplates calibration paths that can act as either "calibration data paths" or "data paths," and because there is no clear disclaimer or disavowal in the intrinsic

[12]This term appears in claims 1-24 of the '6576 patent.

record, the Court rejects Intel's construction.

Intel argued at the hearing that "the point of the invention is to not take the data path out of service" and, therefore, that Intel's "distinct" limitation should be included in the Court's construction. (*See* Tr. at 147) However, the Court agrees with Future Link that "you can have two different claim elements that are identified separately in the claims that read on the exact same physical structure." (*Id.* at 154) Future Link's argument is supported by the specification's disclosure of a "rotating" embodiment which rotates "the calibration procedure through each of the data paths." ('6576 patent at 3:14-15) In the rotating embodiment, different claim elements may be implemented on the same physical structure over time as the calibration path "rotates through" the data paths. (*Id.* at 6:53-59)

Future Link's construction comports with the plain and ordinary meaning of the claim language, in the context of the intrinsic record. (*See, e.g.*, '6576 patent at 8:29-38) Therefore, the Court will adopt Future Link's proposed construction for this term.

"means for comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths"[13]

Future Link Function: "comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths" Structure: "comparison circuit 230"

[13]This term appears in claim 21 of the '6576 patent.

Intel Function: "comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths" Structure: "comparison circuit 230, including (1) an input connected to a data path and an input connected to a calibration path, or (2) inputs connected to data-receive buffers connected to a data path and a calibration path, respectively"
Court Function: "comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths" Structure: "comparison circuit 230"

The parties agree on the function for this means-plus-function term but disagree about the corresponding structure. Intel argues that the structure is "comparison circuit 230" depicted in Figures 2-2 and 2-4 in the '6576 patent, in addition to this circuit's inputs. Future Link argues that the structure is comparison circuit 230 by itself. The Court agrees with Future Link's proposed construction.

As argued by Future Link, the inputs to the comparison circuit are not required structural elements for the claimed function of ***comparing***. (*See* D.I. 288 at 22) (citing *Northrop Grumman Corp. v. Intel Corp.*, 325 F.3d 1346, 1352 (Fed. Cir. 2003)) Intel's citation to *Apple Inc. v. Samsung Elecs. Co.*, 816 F.3d 788, 813 (Fed. Cir. 2016) is inapposite. In *Apple*, the Federal Circuit found that the included "software" limitation was required for the claimed function of transmitting. (*See id.*) Here, the additional input limitations are ***not*** required to implement the claimed function of comparing.

For the foregoing reasons, the Court will adopt Future Link's proposed construction for this term.

G. '108 Patent

"testing the interconnects"[14]

Future Link "applying test data to one end of an interconnect and observing response data at the other end"
Intel "applying test data to one end of an interconnect and observing response data at another end, in such a way that open circuits and short circuits are detected"
Court "applying test data to one end of an interconnect and observing response data at the other end"

Intel argues that "testing the interconnects" must be done "in such a way that open circuits and short circuits are detected." Intel's primary argument in support of its construction is that the '108 patent expressly defines this disputed term. The Court disagrees with this argument. Intel's alleged definition of this term appears in a portion of the specification that is clearly discussing the prior art "boundary-scan test standard." (*See* D.I. 290 at 22) (citing '108 patent at 2:16-20) As such, the definition applies to the "boundary-scan" prior art but not necessarily to the claimed invention, particularly because the claimed invention is described in various places in the specification as being an "alternative" to an "ordinary boundary-scan." (*See, e.g.*, '108 patent at 6:15-19) Intel's purported definition is immediately followed in the specification by a paragraph that criticizes the "boundary-scan" prior art, further signaling a departure by the claimed invention from the prior art. Because Intel's purported definition is not clearly related to the claimed invention, and is not otherwise supported by the intrinsic evidence, the Court rejects Intel's construction.

Future Link's construction is taken from a paragraph of the specification that is

[14]This term appears in claims 1-13 of the '108 patent.

discussing the claimed invention. (*See* D.I. 288 at 23) (citing '108 patent at 2:39-41) Moreover, Future Link's construction is consistent with the rest of the intrinsic evidence, which describes how interconnect testing may generally be accomplished in the various embodiments disclosed in the specification. (*See generally* '108 patent at 5:41-12:43)

For the foregoing reasons, the Court will adopt Future Link's proposed construction for this term.

H. '302 Patent

"functional block" / "module(s)"[15]

Future Link "a combination of components that perform a given function"
Intel "a combination of components that perform a given function, such as a core"[16]
Court "a combination of components that perform a given function"

Intel proposes that "a core" should be included in the Court's construction of this term as an example of a "functional block" or "module." Future Link argues that this example could be confusing to a jury because, *inter alia*, the word "core" is described in at least one part of the specification as only ***part*** of a module rather than as a module itself. (*See* D.I. 315 at 22-23) (citing '302 patent at 4:28-29) The Court agrees with Future Link. Including the "core" example in the Court's construction could unduly draw jurors' attention to the example and could confuse the jury in light of the different uses of the word "core" in the specification.

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[15]This term appears in claims 1-39 of the '302 patent.

[16]At the hearing, Intel argued, for the first time, that this term is indefinite. (*See* Tr. at 174-77)

For the foregoing reasons, the Court will adopt Future Link's proposed construction for this term.

I. '257 Patent

"block"[17]

Future Link "a combination of components that perform a given function"
Intel "a circuit assemblage that functions as a unit"
Court "a component that performs a given function or a combination of components that perform a given function"

The parties' dispute with respect to this term appears to be whether a "block" is a ***singular*** "circuit assemblage" or whether it can be a combination of (potentially disparate) components. (*See* D.I. 290 at 25; D.I. 315 at 27-28) The '257 patent does not define this term. The term is always preceded by the word "secure" in asserted claims 1-4.

Intel's proposed construction does little to aid a jury, because it includes technical terms that do not refine the term's meaning. In addition, Intel's construction appears to be contrary to the specification's description of a "secure block" as potentially comprising multiple, disparate components. (*See* '257 patent at 3:16-27)

Future Link proposes the same construction that it proposed for the term "functional block" as used in the '302 patent, discussed above. The '257 patent describes the term "secure block" as a "***functional block*** that provides secure functions." ('257 patent at 3:22-27) (emphasis added) As discussed above, the parties largely agreed to Future Link's proposed

[17]This term appears in claims 1-4 of the '257 patent.

construction of "functional block" as the term was used in the '302 patent. Future Link's definition, although based on extrinsic evidence, accurately describes the term "block" in the context of the '257 patent, which uses the term in a manner similar to how it is used in the '302 patent. (*See id.* at 3:16-27) (describing "secure block" as comprising six components that together "provide[] secure functions") However, the '257 patent also refers to a "secure block" as a ***singular*** component in at least one place. (*See, e.g.*, 3:1-6) Future Link's proposed construction for "functional block" must be modified to take into account a potential "singular component" implementation.

In light of the above, the Court will construe the term "block" to mean "a component that performs a given function or a combination of components that perform a given function."

J. '680 Patent

"packet-based communications" (claim 1) / "communicating packet data" (claim 8)[18]

Future Link Plain and ordinary meaning (defined as "communications based on packets" (claim 1) / "communicating data based on packets" (claim 8))
Intel "communications as packets" / "communicating data as packets"
Court "communications as packets" / "communicating data as packets"

These terms appear in the preambles of the two independent claims that are being asserted from the '680 patent. Intel argues that these terms should be construed to require communications as packets, in claim 1, or communication of data as packets, in claim 8. The Court agrees. The intrinsic evidence establishes that the claims and patent as a whole are

[18]This term appears in claims 1, 2, 7-11, and 13 of the '680 patent.

directed to communication and processing of information ***as packets***. (*See* D.I. 318 at 29 (Intel citing evidence from intrinsic record); *see also generally MySpace,* 672 F.3d at 1256 ("An inventor is entitled to claim in a patent what he has invented, but no more."))

For the foregoing reasons, the Court will adopt Intel's proposed constructions for these terms.

"generating a performance-based communications order" (claim 1) / "performance arbiter configured and arranged to order the packet data" (claim 8)[19]

Future Link Plain and ordinary meaning (defined as "generating a communications order based on desirable performance" (claim 1) / "arbiter configured and arranged to order the packet data based on desirable performance" (claim 8))
Intel "generating a communications order further based on desirable performance characteristics" / "arbiter configured and arranged to order the packet data further based on desirable performance characteristics"
Court "generating a communications order further based on desirable performance characteristics" / "arbiter configured and arranged to order the packet data further based on desirable performance characteristics"

Intel argues that its proposed constructions will clarify that the claims require a communications order that is "further based on desirable performance characteristics." (*See* D.I. 318 at 29-30) Future Link counters that no construction is necessary, because the meaning of these terms is clear from the context of the claims. (*See* D.I. 315 at 29-30) The Court agrees with Intel.

Intel's proposed construction clarifies the claim language in accordance with how the terms appear in the claim language. Specifically, a protocol-based ordering must be applied

[19]This term appears in claims 1, 2, 7-11, and 13 of the '680 patent.

before any further ordering is applied. (*See* '680 patent at 9:5-16, 10:5-19) This ordering is further supported by the specification and prosecution history cited in Intel's briefs. (*See* D.I. 290 at 28-30; D.I. 318 at 29-30) In addition, inclusion of the word "characteristics" is supported by the specification, which makes clear that desirable performance characteristics form the basis for developing rules to achieve desirable performance. (*See* '680 patent at 7:43-51)

For the foregoing reasons, the Court will adopt Intel's proposed constructions for these terms.

III. CONCLUSION

The Court will construe the disputed terms as described above. An appropriate Order follows.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INTEL CORPORATION,	:	
	:	
Plaintiff,	:	
	:	
v.	:	C.A. No. 14-377-LPS
	:	
FUTURE LINK SYSTEMS, LLC,	:	
	:	
Defendant.	:	

ORDER

At Wilmington, this **2nd** day of **August, 2016**:

For the reasons set forth in the Memorandum Opinion issued this date,

IT IS HEREBY ORDERED that the disputed claim terms of U.S. Patent Nos. 5,608,357 ("'357 patent"); 5,754,867 ("'867 patent"); 5,870,570 ("'570 patent"); 6,052,754 ("'754 patent"); 6,317,804 ("'804 patent"); 6,606,576 ("'6576 patent"); 6,622,108 ("'108 patent"); 7,478,302 ("'302 patent"); 7,743,257 ("'257 patent"); and 7,917,680 ("'680 patent") are construed as follows:

"**Buffer memory ... for removing jitter**," as used in claims 1-27 of the '357 patent, means "buffer memory . . . for removing the offset of data transition locations from their ideally clocked positions."

"**Means for selecting an external to internal clock frequency ratio**," as used in claims 1, 2, and 4 of the '867 patent, has a corresponding function of "selecting an external to internal clock frequency ratio" and a structure of "a signal sent to a RESET pin, a RESET pin, a signal sent to a BUS FREQUENCY pin, and a BUS FREQUENCY pin."

"**Identification device select decoder**," as used in claims 1-14, 17-18 of the '570 patent, means "a PCI-compliant decoder that identifies the target of a configuration access."

"**External bus control circuit**," as used in claims 1-3, 5, 7-9, and 14 of the '754 patent, means "circuitry external to circuit blocks, wherein the circuitry is part of an apparatus for providing communication that allows a plurality of circuit blocks to be connected to a wide variety of shared bus standards while the circuit blocks' internal circuitry remains unchanged."

"**Slave port**," as used in claims 1-3, 5, 7-9, and 14 of the '754 patent, means "a port which is capable of responding to a master port by transmitting information, receiving information, or both."

"**Serial port**," as used in claims 1-5, 8, 9, 16-18, 21-24, 26-28, and 40 of the '804 patent, means "a port that transfers information sequentially."

"**Means, responsive to the comparison, for adjusting the transmission time for the calibration path**," as used in claim 21 of the '6576 patent, has a corresponding function of "responsive to the comparison, adjusting the transmission time for the calibration path" and a structure of "time-adjust logic 212, at least one variable-delay circuit 252, and the connections between those elements."

"**Calibration path for data calibration**," as used in claims 1-24 of the '6576 patent, means "a path for passing calibration data between at least two nodes."

"**Means for comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths**," as used in claim 21 of the '6576 patent, has a corresponding function of "comparing a sequence of data over the calibration path relative to a matched sequence of data being passed on one of the multiple paths'

and a structure of "comparison circuit 230."

"**Low complexity memory**," as used in claims 1-13 of the '108 patent, means "memory that does not have to be put through a complex initialization process before it can be accessed and that has simple access protocols without dynamic restrictions."

"**Testing the interconnects**," as used in claims 1-13 of the '108 patent, means "applying test data to one end of an interconnect and observing response data at the other end."

"**Each functional block incorporating one or more monitors operable to produce respective measurement signals indicative of respective operating parameters of the functional block, and a decoder to select from among the one or more monitors**," as used in claims 31-39 of the '302 patent, means "each functional block incorporating: (1) one or more monitors operable to produce respective measurement signals indicative of respective operating parameters of the functional block; and (2) a decoder to select from among the one or more monitors."

"**Functional block**" / "**module(s)**," as used in claims 1-39 of the '302 patent, means "a combination of components that perform a given function."

"**Block**," as used in claims 1-4 of the '257 patent, means "a component that performs a given function or a combination of components that perform a given function."

"**Packet-based communications" (claim 1) / "communicating packet data" (claim 8)**," as used in claims 1, 2, 7-11, 13 of the '680 patent, mean "communications as packets" / "communicating data as packets."

"**generating a performance-based communications order" (claim 1) / "performance arbiter configured and arranged to order the packet data" (claim 8)**," as used in claims 1, 2,

7-11, 13 of the '680 patent, mean "generating a communications order further based on desirable performance characteristics" / "arbiter configured and arranged to order the packet data further based on desirable performance characteristics."

HON. LEONARD P. STARK
UNITED STATES DISTRICT JUDGE