IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

AVM TECHNOLOGIES, LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No. 15-33-RGA

MEMORANDUM OPINION

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ANDREWS, U.S. DISTRICT JUDGE:

Presently before the Court is the issue of claim construction of multiple terms in U.S. Patent No. 5,859,547 ("the '547 patent"). The Court has considered the Parties' Joint Claim Construction Brief. (D.I. 286).[1] The Court heard oral argument on June 21, 2016. (D.I. 301).

I. BACKGROUND

Plaintiff AVM Technologies, LLC filed this patent infringement action against Defendant Intel Corporation on January 12, 2015, alleging that Intel infringes the '547 patent. (D.I. 1). The '547 patent is directed to "[a] dynamic logic circuit that uses substantially constant power and that has substantially constant propagation delay, independent of the number of inputs the dynamic logic circuit contains." ('547 patent, abstract). It contemplates the use of an evaluation transistor to "separate[] a precharge node from the logic block during a precharge clock phase so that the logic block is not charged." (*Id.*). The patent also discloses the use of "[a] delay coupled to the precharge transistor [which] allows the precharge transistor to remain activated during a portion of an evaluation clock phase to overcome any effects of charge-sharing between the precharge node and the dynamic logic block." (*Id.*). Claim 22 is largely representative and reads as follows:

> 22. A dynamic logic circuit, comprising:
>
> a dynamic logic block having *input transistors all coupled in parallel*;
>
> a precharge transistor;
>
> an evaluation transistor *between the dynamic logic block and the precharge transistor*;
>
> a *clock signal node* directly connected to the evaluation transistor for switching the evaluation transistor between active and inactive states; and

[1] All citations to the docket refer to Civil Action No. 15-33-RGA, unless specifically noted otherwise.

a delay coupled to the precharge transistor for delaying *the clock signal* to the precharge transistor with respect to the evaluation transistor.

(*Id.*, claim 22 (emphases added to denote disputed terms)).

AVM previously asserted the '547 patent against Intel in a prior action before this Court, in which the parties agreed upon constructions for various terms and the Court construed several other claim terms. (C.A. No. 10-610-RGA, D.I. 148). In the prior litigation, the Court entered judgment in favor of Intel after AVM was repeatedly unable to muster any admissible evidence to prove damages. (C.A. No. 10-610-RGA, D.I. 283, 294). The parties agree that the previous constructions should remain operative in the present litigation. (D.I. 286 at pp. 7–8).

II. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324) (alteration in original). When construing patent claims, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977–80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (internal quotation marks omitted).

"[T]he words of a claim are generally given their ordinary and customary meaning. . . . [Which is] the meaning that the term would have to a person of ordinary skill in the art in

question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312–13 (citations and internal quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314.

When a court relies solely upon the intrinsic evidence—the patent claims, the specification, and the prosecution history—the court's construction is a determination of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015). The court may also make factual findings based upon consideration of extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317–19 (internal quotation marks omitted). Extrinsic evidence may assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art, and how the invention works. *Id.* Extrinsic evidence, however, is less reliable and less useful in claim construction than the patent and its prosecution history. *Id.*

"A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GMBH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (citation and internal quotation marks omitted).

III. CONSTRUCTION OF DISPUTED TERMS

1. "clock signal" (claims 6, 13, 20–22)[2]

   a. *AVM's proposed construction*: "signal used to synchronize operations in a circuit"

   b. *Intel's proposed construction*: "a signal with a regular period, used for synchronization"

   c. *Court's construction*: "a signal occurring or recurring at a constant rate, used for synchronization"

The dispute as to the term "clock signal" concerns whether a clock signal encompasses any signal that is used to synchronize operations in a circuit or must be a signal occurring at regular intervals. AVM argues for the former construction, mostly by suggesting there is nothing in the intrinsic record that purports to limit clock signals to transmissions with a regular period. (D.I. 286 at pp. 11–12). AVM also contends that the applicant's July 1998 Amendment, distinguishing the Kondoh prior art, demonstrates the applicant's position that a clock signal does not necessarily need to have a regular period, because the applicant did not argue that a specific signal in Kondoh was not a clock signal despite it not appearing to occur at regular intervals. (*Id.* at pp. 10–11). In addition, AVM points to a single dictionary definition of clock pulse and Intel's U.S. Patent No. 5,483,185 as extrinsic evidence to support its construction. (*Id.* at pp. 12–13). Intel points to the figures in the '547 patent and argues that they only depict the clock signal oscillating at regular time intervals. (*Id.* at p. 16). Intel also cites a number of similar figures from the prior art cited on the face of the '547 patent, which it contends depict clock signals as having regular periodicity. (*Id.* at pp. 16–17). Lastly, Intel cites a series of definitions from technical dictionaries and textbooks that it asserts demonstrate the common understanding of a POSA that clock signals must repeat at regular intervals. (*Id.* at p. 18).

[2] The term "clock signal" also appears in the Court's prior constructions of "evaluation transistor" and "precharge transistor," making it relevant to every claim in the '547 patent. (C.A. No. 10-610-RGA, D.I. 148 at 7–10).

The Court will adopt a modified form of Intel's proposed construction. The '547 patent describes the purpose of the clock signal as being to synchronize the timing of the circuit by controlling when the precharge and evaluation transistors are activated and deactivated relative to one another. (*See, e.g.*, '547 patent, col. 1, ll. 31–43; *id.* col. 4, ll. 41–51; *id.* claims 6, 13). In other words, the clock signal tells the circuit when it should be in a precharge phase versus an evaluation phase, by switching between logic high and logic low voltage levels. (*See, e.g.*, *id.* col. 4, ll. 41–43). Aside from this general background, the specification does not define clock signal or otherwise explicitly address the characteristics of a clock signal.[3] In the absence of a lexicographic definition or disavowal of the full scope of the claim term, I think it is fair to say that "clock signal" is used in its ordinary and customary sense as understood by a POSA. The intrinsic record, however, does not provide clear guidance as to the ordinary and customary meaning. Accordingly, I think it is appropriate to consider extrinsic evidence, because clock signal is a "technical word[] . . . not commonly understood," giving rise to a factual dispute in which extrinsic evidence "may help to establish a usage of trade . . . ." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 837 (2015) (citation and internal quotation marks omitted).

The overwhelming weight of timely[4] extrinsic evidence submitted by Intel compels me to make the factual finding that the ordinary and customary meaning of "clock signal" to a POSA in 1996 necessarily includes some sort of limitation requiring regularity. For instance, the OXFORD

[3] I do not find persuasive either party's claims that the various figures depicting clock signals in the intrinsic record—in the '547 patent itself, the prior art it cites, or the Kondoh amendment—conclusively demonstrate whether clock signals need to occur at regular intervals or not. The cited portions of these references do not expressly discuss this regularity characteristic or the lack of it. At best, they merely depict clock signals that appear to be somewhat regular, or in the case of Kondoh, contain an aberration that disrupts the seeming regularity. These figures therefore do not establish a regularity requirement or the lack thereof, because "it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (rejecting an argument that relied on the fact that "the specification contains figures depicting a groove that is wider than the fins" because "figures in a patent are not drawn to scale unless otherwise indicated").

[4] The applicant filed for the '547 patent on December 20, 1996.

DICTIONARY OF COMPUTING (4th ed. 1996) unambiguously explains, under the heading clock signal:

> The clock rate is the frequency, expressed in hertz, at which active transitions of a given clock signal occur. The active transition may be from a low to a high voltage level, or vice versa, but will always be followed *after a fixed time* by an opposite inactive transition. *The clock signal is thus formed as a series of fixed-width pulses having a fixed repetition frequency.*

(D.I. 289-6 at 5 (emphases added)). Indeed, this reference goes on to explain that this "constant rate" is the very feature that allows clock signals to perform the synchronization function in logic circuits. (*Id.* ("Because of its constant rate, a clock signal is used to initiate actions within a sequential logic circuit and to synchronize the activities of a number of such circuits.")). Additional technical dictionaries and textbooks consistently define "clock" and "clock pulses"[5] with regard to regular intervals, constant rates, or periodicity. (*See, e.g.*, D.I. 289-6 at 9, THE PENGUIN DICTIONARY OF ELECTRONICS (2d ed. 1988) ("The regular pulses applied to the elements of a logic circuit to effect logical operations are called clock pulses."); *id.* at 13, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY (1992) (defining "clock pulses" as "a train of signals in which the separation between pulses is constant and which serves to synchronize information transfer among computer components" and explaining that a clock "controls timing in a system, generally by generating a steady stream of pulses at a tightly controlled constant rate."); *id.* at 17, MICROSOFT COMPUTER DICTIONARY (2d ed. 1994) (defining "clock" as "[t]he electronic circuit in a computer that generates a steady stream of timing pulses—the digital signals that synchronize every operation"); *id.* at 21, MERRIAM-WEBSTER'S COLLEGIATE DICTIONARY (10th ed. 1993) (defining clock as "a synchronizing device (as in a computer) that produces pulses at regular intervals"); D.I. 289-7 at 4, RABAEY, DIGITAL

[5] AVM admits that "technical dictionaries define a 'clock signal' as being synonymous with 'clock pulse' . . . ." (D.I. 286 at p. 12).

INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE (1996) ("Under ideal circumstances, the clock signal is a periodic step waveform with abrupt transitions between the low and the high values . . . .")). All of these definitions and descriptions arise in the technological context of the invention described in the '547 patent and refer to the synchronizing function that the parties agree the clock signal performs.

In the face of these numerous pieces of consistent extrinsic evidence suggesting clock signals recur at regular intervals, AVM is only able to muster one dictionary definition and several examples of what it describes as non-periodic clock signals. While AVM does cite a technical dictionary defining "clock pulse"—which the reference says is "[a]lso called clock signal"—as merely "[t]he signals which are utilized to synchronize the operations of a circuit," AVM ignores the definition of "clock" on the very same page which makes clear that these pulses are emitted in a "steady stream." (D.I. 287-2 at 21, WILEY ELECTRICAL AND ELECTRONICS ENGINEERING DICTIONARY (2004)). I also do not find persuasive AVM's citations to diagrams of gated clocks, clock output signals, or On-Die Clocks that appear non-periodic, as they appear to be referring to something other than a straightforward clock signal. (D.I. 286 at pp. 23–25). In these references, the signals labeled simply as clock signals appear to have a constant rate. (*See, e.g.*, D.I. 288-1 at 39). Moreover, most of these references are dated well after the filing date of the '547 patent. (*See, e.g.*, D.I. 288-3 at 2 (2007); D.I. 288-1 at 35 (2005)).

After reviewing the extrinsic evidence submitted by both parties, I find that "clock signal" should be construed to reflect the fact that the signals must occur at regular intervals in order to synchronize the circuits. I will not, however, employ the exact language from Intel's

proposed construction.[6] Instead, I will opt for language actually used in the extrinsic evidence forming the basis of my *Teva* factual findings: "a constant rate." (D.I. 289-6 at 5; *id.* at 13). Accordingly, I will construe the term "clock signal" to mean "a signal occurring or recurring at a constant rate, used for synchronization."

2. "clock signal node" (claims 6–7, 12–13, 22)

   a. *AVM's proposed construction*: "point on a circuit for receiving a clock signal"

   b. *Intel's proposed construction*: "a node that provides a clock signal to both the precharge transistor and the evaluation transistor"

   c. *Court's construction*: "a point on a circuit that a clock signal passes through on its way to both the precharge transistor and the evaluation transistor"

Terms 2 and 3 present related disputes that revolve around one central contention: whether the same clock signal must go to both the precharge transistor and the evaluation transistor. AVM's overarching contention is that Intel's constructions for Terms 2 and 3 are classic attempts to improperly read a preferred embodiment into the claims. (D.I. 286 at pp. 33–34, 37–39). Moreover, AVM argues, citing the declaration of its expert and a textbook, that "it is beyond reasonable argument that dynamic circuits can have different clock signals connected to the precharge and evaluation transistors (hence a single clock signal node will not 'provide' a clock signal to both transistors)." (*Id.* at p. 40). Intel argues that every embodiment disclosed in the patent requires that the same clock signal, coming from the same clock signal node, be supplied to both the precharge and evaluation transistors. (*Id.* at pp. 35–36). Furthermore, Intel contends that "[t]he key feature of the alleged '547 patent invention—a delay that causes

[6] Despite providing evidence to establish that the ordinary and customary meaning of clock signal encompasses a constant rate or regular intervals, Intel has not provided a single reference using the term "regular period." I think it prudent for a construction based on factual findings to use the terminology actually employed in the relied-upon extrinsic evidence.

simultaneous activation of the precharge and evaluation transistors—cannot be realized if the same clock signal does not go to both the precharge and evaluation transistors." (*Id.* at p. 42).

I agree with Intel. AVM offers no persuasive substantive explanation for how the invention claimed in the '547 patent could function if different clock signals were received by the precharge transistor and evaluation transistor. Instead of offering any substantive explanation for how its construction would operate in the context of the invention described in the patent, AVM simply repeats that the claims should not be limited to the disclosed embodiments. However, read in the context of the '547 patent as a whole and its asserted contribution to the prior art, it is clear to the Court that the '547 patent does not contemplate different clock signals going to the precharge transistor and the evaluation transistor. The clock signal's role in the '547 patent's claimed invention is activating and deactivating the precharge and evaluation transistors, relative to one another:

> A clock signal applied to the clock node 334 switches between logic low and logic high voltage levels, as depicted in FIG. 4A. During an evaluation phase of the clock cycle, the evaluation transistor 306 is activated. As a result, the evaluation transistor 306 electrically couples the precharge node 316 and the logic-block output node 333 so that charge can flow therebetween. During the precharge portion of the clock cycle, the evaluation transistor is deactivated, and the nodes 316 and 333 are electrically uncoupled so that no charge can pass therebetween (except for leakage current through the evaluation transistor).

('547 patent, col. 4, ll. 41–51). The specification discusses the prior art dynamic logic circuits, but notes that they are "generally considered a poor design because charge-sharing between the logic block and the precharge node during the evaluation phase can cause the precharge node to undesirably go low." ('547 patent, col. 2, ll. 32–35). The specification further states that an object of the invention "is to provide a circuit that overcomes charge-sharing that occurs between the logic block and the precharge node." (*Id.* col. 2, ll. 59–61).

The abstract of the patent states that the invention solves this problem occurring in the prior art by employing "[a] delay coupled to the precharge transistor [which] allows the precharge transistor to remain activated during a portion of an evaluation clock phase to overcome any effects of charge-sharing between the precharge node and the dynamic logic block." ('547 patent, abstract). The specification describes an important structural configuration of the invention: placing a delay between the clock signal node and the precharge transistor, which delays the clock signal to the precharge transistor relative to the evaluation transistor. (*Id.* col. 5, ll. 12–13 ("The delay 308 is coupled between the gate 312 of the precharge transistor 302 and the clock node 334.")). The specification repeatedly explains that this structural configuration overcomes the charge-sharing problems of the prior art by creating a brief period where both the precharge transistor and the evaluation transistor are simultaneously activated, allowing the precharge transistor to charge the dynamic logic block. (*Id.* col. 5, ll. 13–16 ("The delay 308 delays the clock signal so that the signal at the gate 312 of the precharge transistors receives a phase-shifted clock signal."); *id.* col. 6, ll. 7–26 (explaining that the period of simultaneous activation "overcomes the problems shown in the [prior art] circuit of FIG. 2" because the logic block is charged "during a portion of the evaluation phase to overcome any charge-sharing that occurs at the start of the evaluation phase"); *id.* col. 7, ll. 5–9 ("Because of delay 508, the precharge transistor 502 and evaluation transistor 506 are activated simultaneously for a short period of time during the evaluation phase. This allows the precharge transistor 502 to charge the logic block 504 . . . .")).

The only disclosed embodiments of the present invention (Figures 3A and 5A) depict a delay coupled between a clock signal node and the gate of the precharge transistor. ('547 patent, Fig. 3A; *id.* col. 5, ll. 11–15; *id.* Fig. 5A; *id.* col. 6, ll. 53–55). In other words, the clock signal

reaching both transistors in these embodiments passes through the clock signal node at some point. Perhaps most importantly, the specification consistently refers to "a" single clock signal or "the" clock signal (singular). (*Id.* col. 4, l. 41 ("A clock signal applied to the clock node . . . ."); *id.* col. 5, l. 14 ("delays the clock signal"); *id.* col. 6, l. 6 ("the delayed clock signal"); *id.* claim 13 ("The dynamic logic circuit of claim 12 further including a clock signal coupled to the clock signal node, the clock signal having a precharge phase during which the precharge transistor is activated and the evaluation transistor is deactivated and an evaluation phase during which the evaluation transistor is activated."). The specification does not once refer to, or even arguably contemplate, clock signals (plural).

Moreover, AVM altogether fails to explain how a fundamental feature of the invention—avoiding charge-sharing by using a delay to adjust the clock signal's arrival at the precharge transistor relative to the evaluation transistor—could be accomplished if the precharge transistor and evaluation transistor each received different clock signals from different nodes. *See Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008) ("The claims of the patent must be read in light of the specification's consistent emphasis on this fundamental feature of the invention."). In other words, in light of the clock signal's role of switching the evaluation and precharge transistors on and off at regular intervals, how could employing a delay do anything to create a period of simultaneous activation of the precharge transistor and evaluation transistor if they received different clock signals in the first place?[7] The only construction that "most naturally aligns with the patent's description of the invention" is one contemplating the same initial clock

[7] Even assuming there is a reasonable answer to this question, that answer is certainly not contemplated anywhere in the '547 patent. AVM cannot expand a claim term beyond the scope of the invention actually disclosed in the specification, especially to the extent that the invention could not function as the patent describes. *See Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) ("The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose.").

signal passing through the same clock signal node on its way to both the precharge and evaluation transistors. *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1313 (Fed. Cir. 2007).

Accordingly, the Court construes "clock signal node" as "a point on a circuit that a clock signal passes through on its way to both the precharge transistor and the evaluation transistor."[8]

3. "the clock signal" (as recited in claim 22)

   a. *AVM's proposed construction*: "As used in claim 22, 'the clock signal' refers to a 'clock signal' coupled to the precharge transistor"

   b. *Intel's proposed construction*: "The clock signal at the clock signal node"

   c. *Court's construction*: "The clock signal at the clock signal node"

The parties' dispute as to Term 3 is likely controlled by the Court's construction of Term 2. In any event, I think the proper construction of Term 3, limited to "the clock signal" appearing in the last limitation of claim 22, is even clearer. Intel argues that it must be clarified that "the clock signal" in the final limitation of claim 22 is the same clock signal that is at the clock signal node and going to both the precharge transistor and the evaluation transistor, because otherwise the phrase would have no antecedent basis, despite using the definite article "the." (D.I. 286 at pp. 45–47). AVM contends that the "claim language unambiguously requires that 'the clock signal' in claim 22 be coupled to the precharge transistor and delayed by the 'delay' circuit element." (*Id.* at p. 44). Thus, AVM argues that Intel's "proposal that 'the clock signal' is the signal 'at the clock signal node' improperly attempts to unlink the 'clock signal' from the precharge transistor." (*Id.*).

For the reasons discussed above as to Term 2, I conclude that Claim 22 requires the same clock signal to go to the precharge transistor and the evaluation transistor. Claim 22 makes this

[8] In order to avoid any ambiguity, I decline to adopt the "provide" language suggested by Intel. I think the clock is what actually generates and provides the clock signal. The Court's construction reflects the clock signal node's role as a point on the circuit that serves as a pass through point before the clock signal reaches both the precharge and evaluation transistors.

even clearer than the specification, by using the definite article "the" to denote a single clock signal and expressly stating that the "delay coupled to the precharge transistor [is for] delaying the clock signal to the precharge transistor *with respect to the evaluation transistor*." ('547 patent, claim 22 (emphasis added)). Thus claim 22 captures the fact that the function of the delay element is to delay the clock signal's arrival at the precharge transistor, thereby creating a short period where the precharge transistor and evaluation transistor are simultaneously activated. Claim 22 is also perfectly consistent with the descriptions of the invention in the specification, in that it describes the clock signal node being directly connected to the evaluation transistor but only the delay being directly connected to the precharge transistor, because the delay is between the clock signal node and the precharge transistor.

Accordingly, the Court will construe "the clock signal," as used in claim 22, to mean "the clock signal at the clock signal node."

4. "between the dynamic logic block and the precharge transistor" (claims 1, 19, 22).

   a. *AVM's proposed construction*: No construction necessary. But if construed, "somewhere intermediate the dynamic logic block and the precharge transistor"

   b. *Intel's proposed construction*: "positioned to electrically isolate the precharge node from the logic block"

   c. *Court's construction*: "positioned such that the only way charge can flow from the precharge transistor to the logic block is by passing through the evaluation transistor"

AVM argues that "between" has a well-understood meaning that is "clearer and more succinct than any definition," and that the '547 patent never redefines or limits the term to require "electric isolation." (D.I. 286 at pp. 50–51). AVM further contends that Intel's proposed construction would result in the term "between" having different meanings in different areas throughout the same patent. (*Id.* at p. 51). Lastly, AVM argues that Intel is improperly

attempting to read a limitation from the preferred embodiment into the claims. (*Id.* at pp. 52–53). Intel argues that the specification repeatedly explains that the positioning of the evaluation transistor between the precharge transistor and the logic block "allows the evaluation transistor to electrically uncouple—and thus isolate—the precharge node from the logic block, preventing charge from flowing from the precharge node 316 to the logic block 304 (except when desired during the evaluation phase)." (*Id.* at p. 54). Intel also points out that in the previous litigation, AVM argued for "evaluation transistor" to be construed similarly to what Intel proposes here, a "transistor that functions to isolate the precharge node from the logic block." (*Id.* at p. 55). Intel also asserts that "between" cannot simply be given its plain and ordinary meaning, because "one of AVM's . . . infringement theories would allow an alleged 'evaluation transistor' to be positioned so that it cannot electrically isolate the precharge node from the logic block." (*Id.* at pp. 55–56).

It is clear from a full reading of the '547 patent that a fundamental feature of the invention is that the evaluation transistor separates and isolates the logic block from the precharge node. The first sentence of the abstract describes the invention as "[a] dynamic logic circuit that uses substantially constant power and that has substantially constant propagation delay, independent of the number of inputs the dynamic logic circuit contains." ('547 patent, abstract). The abstract then states that the evaluation transistor's positioning between the precharge node and the logic block is what allows for these features of the invention. (*Id.* ("The evaluation transistor separates a precharge node from the logic block during a precharge clock phase so that the logic block is not charged. . . . Because the evaluation transistor separates the logic block from the precharge node, the precharge node can be charged independently of the number of inputs present in the dynamic logic block.")). Moreover, the specification repeatedly

explains that these advantages, which are improvements over the prior art, can be achieved because the evaluation transistor isolates the precharge transistor from the logic block:

> The circuit according to the invention has several advantages. The precharge transistor is isolated from the logic block by the evaluation transistor. Consequently, as the number of inputs of the logic block increases, the precharge transistor is unaffected by any increase in capacitance of the logic block. Moreover, the electrical uncoupling of the precharge node from the logic block allows the precharge transistor to be a constant size regardless of the number of inputs the circuit contains. The precharge transistor only needs to be large enough to charge the precharge node. Still further, power is also saved by only charging the precharge node during the precharge phase, rather than the precharge node and the logic block.

('547 patent, col. 3, ll. 27–39; *see also id.* col. 7, ll. 33–41; *id.* col. 7, ll. 49–55 ("The circuit has substantially constant propagation delay, independent of the number of inputs the circuit contains. This is also the result of separation of the dynamic logic block from the precharge node."); *id.* col. 7, ll. 60–67 (explaining that "[t]he precharge transistor can be sized smaller than precharge transistors in prior circuits" and "can stay substantially the same size regardless of the number of inputs the circuit contains," "because of the isolation of the precharge node from the logic block during the precharge phase")). Moreover, the block-quoted portion of the specification above, prefaced by "according to the invention," makes clear that the advantages resulting from the evaluation transistor's positioning apply to the invention as a whole, rather than just a specific embodiment. *See Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent [] describes the features of the 'present invention' as a whole, this description limits the scope of the invention.").

At oral argument, counsel for Intel indicated that a key aspect of the parties' dispute is whether there can be another path for charge to flow between the precharge node and the logic block that does not pass through the evaluation transistor. (D.I. 301 at 85–86). The specification makes sufficiently clear that the evaluation transistor's important function is to electrically

couple and uncouple (or isolate) the precharge node and the logic block—depending upon the phase indicated by the clock signal—so that charge either can or cannot flow in between the two circuit elements. ('547 patent, col. 4, ll. 41–51; *see also id.* col. 6, ll. 1–3 ("The evaluation transistor electrically uncouples the logic block and the precharge node (so substantially no charge flows therebetween).")). Electrically coupling and uncoupling is the function of the evaluation transistor, and I conclude that it need not be read into the construction of the disputed phrase describing its location. (*Id.* col. 3, ll. 9–11 ("An evaluation transistor is positioned between the logic block and the precharge transistor *and* electrically uncouples the logic block from the precharge node . . . ." (emphasis added))). However, I think it is equally clear that a necessary condition of the evaluation transistor being able to prevent charge from flowing to the logic block is a structural limitation, applied to the circuit as a whole, requiring that there are no other pathways for charge to flow between the precharge node and the logic block. Otherwise, the specification's numerous discussions of the evaluation transistor's isolating role, and the accompanying advantages such isolation provides over the prior art, would be rendered meaningless. That should not be the case, because the evaluation transistor's isolating role is a fundamental feature of the invention described in the '547 patent. *See Praxair,* 543 F.3d at 1324.

Put more simply, the invention would not be able to function as consistently described in the specification if there were pathways between the precharge node and logic block that do not go through the evaluation transistor. While the specification suggests that "the embodiment can be modified in arrangement and detail without departing from such principles" ('547 patent, col. 8, ll. 9–11), construing the claims of the '547 patent as broadly as AVM proposes would constitute a wholesale departure from the principles set forth in the specification. Such a construction would be improper. *See Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1370

(Fed. Cir. 2003) ("[W]here the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims.").

Accordingly, the Court will construe "between the dynamic logic block and the precharge transistor" to mean "positioned such that the only way charge can flow from the precharge transistor to the logic block is by passing through the evaluation transistor."

5. "input transistors" (claims 19, 22)

a. *AVM's proposed construction*: No construction necessary. But if construed, "transistors that can be arranged to provide a logic function."

b. *Intel's proposed construction*: "two or more transistors each capable of independently receiving a different gate input signal"

c. *Court's construction*: No construction necessary.

Intel seeks to limit the term "input transistors" to reflect its contention that "input transistors were "well known in the art as devices capable of independently receiving different input signals." (D.I. 286 at p. 64). Intel seeks to include this narrowing limitation by citing the figures in the '547 patent that depict different input signals going to each transistor in the logic block, similar figures in other patents, and the declaration of its expert, Dr. Subramanian. (*Id.* at pp. 64–66). The core of Intel's argument, however, is that AVM's infringement contentions "seek[] to read the term 'input transistors' (plural) to cover a single device that is capable of receiving only a single input signal." (*Id.* at pp. 66–67). AVM responds that it "agrees that multiple transistors are required, which is why AVM's construction includes the plural, 'transistors.'" (*Id.* at p. 67). AVM also asserts—citing its expert, Dr. McAlexander—that Intel only "point[s] to patents and textbooks that show examples of transistors receiving different inputs. But it was also well known in the art that transistors, including input transistors in a

dynamic logic block, will often be configured to receive only the same signal." (*Id.* at p. 70 (citing D.I. 296-5 at 72–76, ¶¶ 24–32)).

I agree with AVM that no construction is necessary. Intel does not point to any intrinsic evidence demonstrating that the meaning of input transistors, in the context of the patent, is limited to only those that are "each capable of independently receiving a different gate input signal." Moreover, Intel does not muster any convincing extrinsic evidence that such a limitation was part of the known meaning of the term in the art. Intel merely cites figures depicting input transistors each receiving a separate signal and the bald assertions of its expert. Indeed, Intel even concedes that "the patent allows multiple transistors to receive the same signal" and that "input transistors are 'transistors that can be arranged to provide a logic function.'" (D.I. 286 at pp. 64, 66). At bottom, the parties' dispute actually appears to be over whether the input transistor component of one of the accused products, a FinFET structure, should be characterized as a single input transistor or multiple input transistors. (D.I. 286 at p. 70; D.I. 296-5 at 77–81, ¶¶ 36–41; D.I. 298-7 at 30–31, ¶¶ 107–08). Yet the parties agree on the basic function of input transistors and that the claims require multiple input transistors. Whether a particular accused product has one input transistor or multiple input transistors is a fact question for a jury to decide. Intel has thus failed to show that its proposed limitation is warranted as a matter of claim construction. Given this determination, and in order to resolve the parties' "fundamental dispute regarding the scope of a claim term," I conclude that Intel may not argue later on that the term "input transistors" requires that each transistor be independently capable of receiving a different gate input signal. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

6. "input transistors all coupled in parallel" (claim 22)

   a. *AVM's proposed construction*: "input transistors whose source nodes are connected together, directly or through other elements, and whose drain nodes are connected together, directly or through other elements"

   b. *Intel's proposed construction*: "two or more input transistors having their sources directly connected to a first common node and their drains directly connected to a second common node"

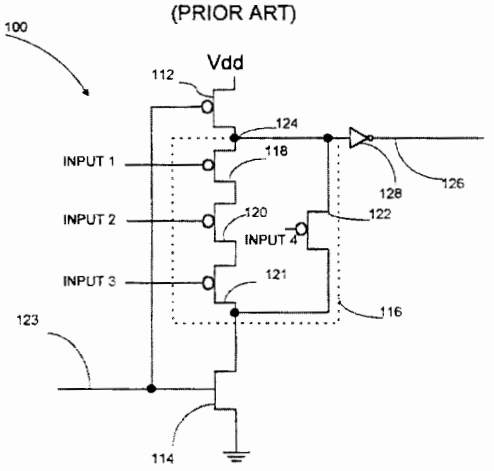
   c. *Court's construction*: "two or more input transistors having their sources directly connected to a first common node and their drains directly connected to a second common node"

This dispute concerns whether the term "input transistors all coupled in parallel" requires that these transistors have their sources all directly connected to a common node and their drains all directly connected to a second common node, or whether two transistors are still coupled in parallel if their sources and drains are only indirectly connected to a common node via other input transistors. (D.I. 286 at pp. 72–74). AVM argues that the term "encompasses both direct and indirect connections." (*Id.* at p. 72). First, it asserts that the parties' previously agreed-upon construction of "coupled to" from the prior litigation to mean "connected, directly or through intervening elements," is dispositive as to the present dispute. (*Id.*). Second, AVM contends that Figure 1A of the '547 patent, and the specification's description of input transistor 122 being coupled in parallel across the other input transistors (118, 120, 121), demonstrate that Intel's construction cannot be correct. (*Id.* at p. 73). Third, AVM points to Figure 4 of U.S. Patent No. 5,453,708 as supporting its construction, because the patent describes the transistors shown in Figure 4 as being in both "serial and parallel arrangements," even though "none of the input transistors 29 have their sources directly connected to a first common node and their drains directly connected to a second common node." (*Id.* (internal quotation marks omitted)).

Intel argues, citing Figures 1A and 3D of the '547 patent and the accompanying descriptions in the specification, that the '547 patent uses the term "in parallel" in its ordinary, conventional manner. (*Id.* at p. 75). Intel seeks to establish the ordinary and customary meaning of "in parallel" in the electrical engineering field by reference to a number of technical dictionaries. (*Id.* at p. 74). Based on these two premises, Intel contends that "in parallel" requires that each transistor be directly connected to two common nodes, while "in series" allows two or more transistors to be connected to the nodes indirectly through other elements. (*Id.* at p. 76). Intel also points to prior art references cited by the '547 patent as confirming the distinction between transistors coupled in parallel and in series. (*Id.*).

The Court will adopt Intel's construction. Figure 1A of the '547 patent, showing a prior art dynamic logic circuit, appears as follows:

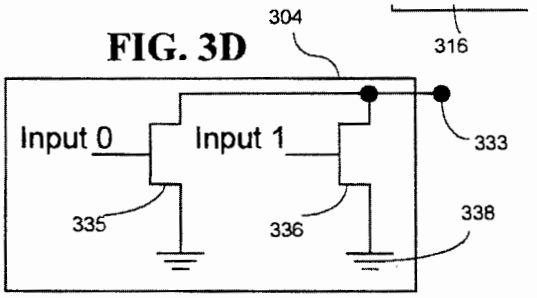
FIG. 1A
(PRIOR ART)



Referencing Figure 1A, the specification explains that: "Logic block 116 has a group of three input transistors 118, 120, 121 coupled in series and one input transistor 122 coupled in parallel across the other input transistors." ('547 patent, col. 1, ll. 26–30). Thus, the patent describes transistors 118, 120, and 121 as being coupled in series; they are only connected to common nodes indirectly, through their connections to the other transistors in the series. Intel's explanation that "input transistor 122 is connected in parallel with the combination of input

transistors 118, 120, and 121" (D.I. 286 at p. 76) is consistent with the specification's description of transistor 122 being "coupled in parallel across the other input transistors."

Figure 3D of the '547 patent also shows "an example of a logic block 304." ('547 patent, col. 4, ll. 56–57). Figure 3D appears as follows:



The specification explains that "FIG. 3D shows the input transistors [335 and 336] as being N-channel transistors coupled in parallel . . . ." (*Id.* col. 5, ll. 3–4). It also explains that they are "coupled between the logic-block output node 333 and a negative supply voltage, in this case, ground 338." (*Id.* col. 4, ll. 59–61). The specification goes on to explain that, "Additionally, the transistors can be arranged all in parallel, all in series, or a series/parallel combination." (*Id.* col. 5, ll. 6–8). Thus Figure 3D and the accompanying descriptions in the specification do three important things. First, they show an explicit example of transistors coupled in parallel that comports with Intel's construction. Second, they indicate that being coupled in series versus coupled in parallel represents a distinct difference. Third, the "series/parallel combination language" validates Intel's explanation that a transistor can be coupled in parallel across a combination of transistors that are coupled in series.

Furthermore, what I find significant about AVM's proposed construction is that it renders the phrase "in parallel" practically meaningless. AVM's proposed construction is more or less the same as the parties agreed-upon construction for "coupled to" ("connected, directly or through intervening elements"), rendering the phrase "in parallel" inconsequential. (D.I. 287-2

at 5). Yet such an interpretation would be inconsistent with the specification's teachings that there are differences between being coupled in series and coupled in parallel. *See Phillips*, 415 F.3d at 1313 ("[T]he [POSA] is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification."). AVM's construction also would render transistors 118, 120, and 121 from Figure 1A in parallel, even though the specification expressly states that they are in series with one another. ('547 patent, col. 1, ll. 26–30). Intel's construction is also consistent with other intrinsic evidence. Figures and descriptions appearing in prior art references cited by the '547 patent, including U.S. Patent Nos. 5,402,012 and 5,453,708, distinguish between being coupled in parallel and coupled in series. (D.I. 289-4 at 3 ('012 patent, Fig. 2), at 10 ('012 patent, col. 5, ll. 38–48); D.I. 287-1 at 73–74 ('708 patent, Figs. 2–4), at 81 ('708 patent, col. 2, ll. 42–50), at 82 ('708 patent, col. 4, ll. 54–57)).

At bottom, AVM fails to propose a construction that would give any meaning to the phrase "in parallel," instead only providing vague explanations as to why Intel's construction is improperly limiting. I find AVM's arguments unconvincing and at odds with basic principles of claim construction.[9] *See Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim.").

[9] I do not think it is necessary to resort to extrinsic evidence in construing this term, in light of the intrinsic record. To the extent it would be relevant to do so, I note that Intel submitted textbooks and technical dictionaries, although dated well after the patent's filing date, which provide definitions that are consistent with its proposed construction. (*See, e.g.*, D.I. 289-6 at 25, THE AMERICAN HERITAGE SCIENCE DICTIONARY (2005) ("Circuits in which a power source is connected to two or more components (such as light bulbs, or logic gates in a computer circuit, one after the other, are called series circuits. . . . Circuits in which a power source is directly connected to two or more components are called parallel circuits."); D.I. 290-2 at 22, MAZMUDER, INTRODUCTION TO ENGINEERING: AN ASSESSMENT AND PROBLEM SOLVING APPROACH (2016) ("Components in parallel have the terminals directly connected to the main node in a circuit. This form of configuration allows multiple pathways for charge to flow.")). AVM, on the other hand, does not cite any extrinsic evidence.

Accordingly, the Court will construe "input transistors all coupled in parallel" to mean "two or more input transistors having their sources directly connected to a first common node and their drains directly connected to a second common node."

IV. CONCLUSION

Within five days the parties shall submit a proposed order consistent with this Memorandum Opinion suitable for submission to the jury.