**IN THE UNITED STATES DISTRICT COURT**
**FOR THE DISTRICT OF DELAWARE**

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| ALTAIR LOGIX LLC, | ) | |
| | ) | |
| Plaintiff, | ) | |
| | ) | |
| v. | ) | Civil Action No. 20-1004-MN-CJB |
| | ) | |
| NETGEAR, INC., | ) | |
| | ) | |
| Defendant. | ) | |

**REPORT AND RECOMMENDATION**

Pending before the Court in this patent infringement case is Defendant Netgear, Inc.'s ("Netgear" or "Defendant") "Motion for Judgment on the Pleadings of Invalidity Under 35 U.S.C. § 101[,]" filed pursuant to Federal Rule of Civil Procedure 12(c) (the "Motion"). (D.I. 50) With the Motion, Netgear seeks an order declaring claim 1 of United States Patent No. 6,289,434 (the "'434 patent") invalid for failure to claim patent eligible subject matter. For the reasons that follow, the Court recommends that Netgear's Motion be DENIED.

## I. BACKGROUND

### A. Factual Background

The '434 patent is entitled "Apparatus and Method of Implementing Systems on Silicon Using Dynamic-Adaptive Run-Time Reconfigurable Circuits for Processing Multiple, Independent Data and Control Streams of Varying Rates." (D.I. 1, ex. A (hereinafter, "'434 patent")) It was issued on September 11, 2001 from U.S. Appl. No. 09/032,530, which was filed on February 27, 1998. (*Id*.) The invention relates to the field of "runtime reconfigurable dynamic-adaptive digital circuits [that] can implement a myriad of digital processing functions related to systems control, digital signal processing, communications, image processing, speech and voice recognition or synthesis, three-dimensional graphics rendering[ and] video

processing." (*Id.*, col. 1:31-38) The object of the invention is to provide a new apparatus for implementing systems on chips that enable a user to achieve the "performance of fixed-function implementations at a lower cost." (*Id.*, cols. 2:64-3:1)

The "Background of the Invention" section describes four prior art ways of implementing various functions on an integrated circuit. The most common method entails specifically designing the functions to be performed by "placing on silicon an interconnected group of digital circuits in a non-modifiable manner (hard-wired or fixed[-]function implementation)." (*Id.*, col. 1:42-47) The circuits are designed to provide the fastest possible operation of the circuit in the least amount of silicon area. (*Id.*, col. 1:47-49) These circuits are comprised of an interconnection of various amounts of random access memory and logic circuits. (*Id.*, col. 1:49-51) Complex systems on silicon are broken up into separate blocks, with each block designed separately to perform solely the function that it was intended to perform. (*Id.*, col. 1:51-54) Each block has to be individually tested and validated, and then the entire system must be tested. (*Id.*, col. 1:54-56) The patent explains that this method was the "smallest (i.e., cheapest in terms of silicon area)" among the four prior art methods of implementing such systems, but that it was also "becoming increasingly complex[.]" (*Id.*, col. 1:57-65) This method is also the best performing method of the prior art methods. (*Id.*, col. 2:34-38)

The second prior art method entails utilizing software with a microprocessor and an associated computing system. (*Id.*, col. 2:1-2) However, the patent explains that this system cannot deliver real-time performance in a cost-effective manner. (*Id.*, col. 2:3-5) The use of this system is best for modeling the subsequent hard-wired/fixed-function system before significant design effort is put into the system design. (*Id.*, col. 2:5-8)

The third prior art method of implementing various functions on an integrated circuit is by using a digital signal processor ("DSP"), which is a class of computing machines that are useful for real-time processing of various speech, audio, video and image processing problems. (*Id.*, col. 2:9-12) However, the patent notes that the use of DSPs are not cost-effective for performing tasks that do not have a high degree of parallelism in them, nor for performing tasks requiring multiple parallel threads of operations (such as three-dimensional graphics). (*Id.*, col. 2:14-17)

The fourth way of implementing such systems is by using field programmable gate arrays ("FPGAs"). (*Id.*, col. 2:18-19) FPGAs are devices consisting of a two-dimensional array of fine grained logic and storage elements that can be connected together in the field by downloading a configuration stream that routes signals between these elements. (*Id.*, col. 2:19-23) While the patent notes that utilizing FPGAs provides a greater flexibility for optimizing the silicon usage in such devices, that flexibility comes with an increased cost and a decrease in performance. (*Id.*, col. 2:26-33)

The second, third and fourth systems could theoretically be cheaper to implement by removing redundancy from the system, which can be accomplished by reusing computational blocks and memory. (*Id.*, col. 2:39-41) However, these systems are increasingly complex, and thus their computational density is very high when compared with fixed-function implementations (i.e., the first prior art method described). (*Id.*, col. 2:42-44) As for fixed-function systems, they must include blocks designed to implement all possible functional requirements of the required data processing—regardless of the final application of the device or the nature of the data. (*Id.*, col. 2:53-57) Accordingly, if a fixed-function implementation is

required to adaptively process data, it has to commit silicon resources to process all possible types of data. (*Id.*, col. 2:58-60)

The inventor of the '434 patent set out to provide a new apparatus for implementing systems on silicon that will enable the user to achieve the performance of fixed-function implementation at a lower cost. (*Id.*, cols. 2:64-3:1) The specification explains that cost is reduced by removing redundancy from the system, which is turn achieved by re-using groups of computational and storage elements in different configurations. (*Id.*, col. 3:2-4) The cost is further reduced by utilizing only static or dynamic random access memory as a means for maintaining the state of the system. (*Id*., col. 3:4-6) The invention purportedly provides a way to effectively adapt the configuration of the circuit to different input data and processing requirements. (*Id.*, col. 3:6-8) This reconfiguration can take place dynamically in run-time without any decrease in performance over fixed-function implementations. (*Id.*, col. 3:8-11)

The "Summary of the Invention" section of the specification explains that an apparatus is provided "for adaptively dynamically reconfiguring groups of computational and storage elements in run-time to process multiple separate streams of data and control at varying rates. The aggregate of the dynamically reconfigurable computational and storage elements will heretofore be referred to as a 'media processing unit.'" (*Id.*, col. 3:13-19) The patent states that these media processing units constitute the "heart" of the claimed architecture. (*Id.*, col. 13:4-5) And the specification further explains that the media processing units include "execution units" consisting of a multiplier, an arithmetic unit, an arithmetic logic unit and a bit manipulation unit. (*Id.*, cols. 16:15-23:35)

The '434 patent recites a single claim:

> **1**. An apparatus for processing data, comprising:

an addressable memory for storing the data, and a plurality of instructions, and having a plurality of input/outputs, each said input/output for providing and receiving at least one selected from the data and the instructions;

a plurality of media processing units, each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs and comprising:

a multiplier having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output;

an arithmetic unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output;

an arithmetic logic unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with at least one selected from the multiplier and arithmetic unit; and

a bit manipulation unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with the arithmetic logic unit and at least one selected from the multiplier and arithmetic unit;

each of the plurality of media processors for performing at least one operation, simultaneously with the performance of other operations by other media processing units, each operation comprising:

receiving at the media processor input/output an instruction from the memory;

receiving at the media processor input/output data from the memory;

processing the data responsive to the instruction received to produce at least one result; and

providing at least one of the at least one result at the media processor input/output.

(*Id.*, cols. 55:21-56:33)

Additional relevant facts about the '434 patent will be set out below in Section III.

### B. Procedural Background

Altair filed this case on July 28, 2020, alleging that Netgear's Meural 27" digital photo frame infringes claim 1 of the '434 patent. (D.I. 1 at ¶ 26)[1] Netgear filed the instant Motion on August 13, 2021, (D.I. 50), which was fully briefed as of September 24, 2021, (D.I. 58). A *Markman* hearing is scheduled for February 23, 2022. (D.I. 30 at ¶ 14)

## II. STANDARD OF REVIEW

In evaluating a motion for judgment on the pleadings brought pursuant to Federal Rule of Civil Procedure 12(c) ("Rule 12(c)"), the Court must view all factual allegations in a complaint in the light most favorable to the non-moving party. *See Wolfington v. Reconstructive Orthopaedic Assocs. II PC*, 935 F.3d 187, 195 (3d. Cir. 2019). This is the same standard that applies to a motion to dismiss brought pursuant to Federal Rule of Civil Procedure 12(b)(6). *Id.* A Rule 12(c) motion will not be granted "unless the movant clearly establishes that no material issue of fact remains to be resolved and that he is entitled to judgment as a matter of law." *Id.* (internal quotation marks and citation omitted). In deciding such a motion, the Court may consider only the pleadings, the exhibits attached thereto, matters of public record and undisputedly authentic documents integral to the pleadings. *Id.*

[1] This case has been referred to the Court by United States District Judge Maryellen Noreika to hear and resolve all pretrial matters, up to and including expert discovery matters. (D.I. 10)

The instant Rule 12(c) Motion asserts that claim 1 of the '434 patent is directed to patent-ineligible subject matter—i.e., it avers that dismissal is warranted due to the presence of an affirmative defense. The Court has often set out the relevant legal standards for review of this type of Section 101-related motion at the pleading stage, including in *Genedics, LLC v. Meta Co.*, Civil Action No. 17-1062-CJB, 2018 WL 3991474, at *2-5 (D. Del. Aug. 21, 2018). The Court hereby incorporates by reference its discussion in *Genedics* of these legal standards and will follow the standards herein. To the extent consideration of Netgear's Motion necessitates discussion of other, related legal principles, the Court will set out those principles in Section III below.

## III. DISCUSSION

In *Alice*'s first step, the Court must determine whether claim 1 is "directed to" a patent-ineligible concept (here, an abstract idea). *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 217 (2014). The "'directed to' inquiry applies a stage-one filter to claims, considered in light of the specification, based on whether 'their *character as a whole*'" or their "focus" is directed to excluded subject matter. *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335-36 (Fed. Cir. 2016) (quoting *Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1346 (Fed. Cir. 2015) (emphasis added)).

Here, Netgear argues that claim 1 is directed to the abstract idea of "data processing[,]" and that this is so because the claim fails to "recite how the claimed result [of processing data] is achieved in a particularized way or how it arises out of otherwise generic computer components." (D.I. 51 at 1, 8; *see also id.* at 2, 7, 12; D.I. 58 at 1) For its part, Altair does not dispute that "data processing" is an abstract idea. (D.I. 57 at 10) And the Court agrees that it is. *See, e.g.*, *iLife Techs., Inc. v. Nintendo of Am., Inc.*, 839 F. App'x 534, 536 (Fed. Cir. 2021) ("We

have routinely held that claims directed to gathering and processing data are directed to an abstract idea."); *Content Extraction & Transmission LLC v. Wells Fargo Bank, Nat'l Ass'n*, 776 F.3d 1343, 1347 (Fed. Cir. 2014) (concluding that claims were directed to the "abstract idea of 1) collecting data, 2) recognizing certain data within the collected data set, and 3) storing that recognized data in a memory").

But is it right to say that claim 1 is *directed to* just "data processing"? Altair says no. Instead, Altair argues that the claim is directed to something much more specific: to an apparatus: (1) that includes a plurality of media processing units (comprised of execution units that include a multiplier, an arithmetic unit, an arithmetic logic unit and a bit manipulation unit); (2) that allows certain of the execution units to operate concurrently with each other; and (3) that requires the media processing units be connected to addressable memory input/outputs, such that each of the media processing units can simultaneously receive instructions and data from the memory, process the data and output a result with the other media processing units. (D.I. 57 at 10, 13, *see also id.* at 19) For the reasons discussed below, the Court agrees with Altair.

The Court turns first to the specification, which is a useful tool for determining what the patent's claim is directed to. *See Genedics, LLC*, 2018 WL 3991474, at *4. Here, there are portions of the specification that support Altair's position. For example, the specification notes that the invention's use of multiple media processing units is the "heart" of the claimed architecture. ('434 patent, col. 13:4-5) It then explains that each of these media processing units are "made up of very high speed core elements that on a pipelined basis can be configured to form a more complex function[, which] leads to a lower gate count, thereby giving a smaller die size and ultimately a lower cost." (*Id.*, col. 13:26-31) These aspects of the media processing unit are in turn said to help contribute to their "re-configurability and re-usability[,]" (*id*., col.

13:26-27), which in turn is said to help remove redundancy and reduce cost, (*id*., cols. 2:64-3:11).[2] The specification also calls out the importance of the fact that various of the execution units can "work concurrently during an execution phase." (*Id*., col. 24:38-62) And it discusses the importance of the media processing units being able to work simultaneously, such as when it describes how the apparatus can process data "in series or in parallel[.]" (*Id*., Abstract; *see also id*., cols. 13:5-9, 54:54-62); *Nw. Univ. v. KUKA AG*, Case No. 21 C 599, 2021 WL 4711538, at *4 (N.D. Ill. Oct. 8, 2021) (explaining that certain provisions in the specification "suggest that what the claims are directed to is the intelligent assist system's modular architecture" and not simply the proposed abstract idea, which was "network communication for device interaction").

These aspects of the invention are also prominently referenced in claim 1. The claim requires that the apparatus referred to therein must be comprised of particular components—including the multiple media processing units, which in turn must be comprised of a multiplier, an arithmetic unit, an arithmetic logic unit and a bit manipulation unit. ('434 patent, cols. 55:27-56:20) It further dictates that certain of these execution units must be capable of operating concurrently, (*id.*, col. 56:6-20), and that the plurality of multiple media processing units themselves must be able to perform operations simultaneously with each other, (*id.*, col. 56:21-33). (D.I. 57 at 12); *see also Visual Memory LLC v. NVIDIA Corp.*, 867 F.3d 1253, 1260 (Fed. Cir. 2017) (rejecting the defendant's assertion that the claims were directed to no more than a desired result in the context of generic computer components, where even the broadest claim "requires a memory system with a main memory and a cache memory, where the memory

[2] The specification sets out additional benefits with respect to the media processing units, including that they make writing software very easy because they are virtually identical to one another, and that any one of the media processing units can take on a supervisory role and act as a central controller. ('434 patent, col. 13:32-40)

system is configured by a computer to store a type of data in the cache memory based on the type of processor connected to the memory system").

Netgear's arguments to the contrary—i.e., that claim 1 is not directed to these more particularized aspects of the claim, but instead simply to the general concept of "data processing"—are not persuasive.

For example, in arguing that claim 1 is directed only to "data processing," Netgear simply ignores the computer components that are found in the claim; having done so, Netgear focuses on the remaining portions of the claim language, in order to justify the appropriateness of its proposed abstract idea. (D.I. 51 at 10-11; *see also id.* at 6) In other words, Netgear highlights the parts of the claim requiring that: (1) the addressable memory *stores* data and certain instructions; and (2) media processing units *receive* an instruction and data, *process* that data, and *provide* at least one result. (*Id*.) By emphasizing these claimed steps of *storing*, or *receiving*, or *processing* or *providing* data, Netgear tries to portray the claim as being focused solely on "functional language" and "result-focused elements[.]" (*Id.* at 10-13)

The problem with that approach, however, is that it leaves out the meat of the claim—i.e., the portions of claim 1 requiring that the apparatus must include multiple media processing units (as well as each of the four types of execution units making up such units), and requiring that those units must work together and with the addressable memory in a certain way. Netgear says that it did so because the claimed computer components and the way they interact with each other are merely "generic" and "employed in the conventional manner." (*Id.* at 6-8; *see also* D.I. 58 at 1-3); *see also In re TLI Commc'ns LLC Patent Litig*., 823 F.3d 607, 612 (Fed. Cir. 2016) (asking, at step one, whether claims were directed to an improvement in the functioning of a computer or, instead, to, *inter alia*, generalized steps to be performed on a computer using

conventional computer activity); *Enfish*, 822 F.3d at 1335-36 (asking, at step one, "whether the focus of the claims is on [a] specific asserted improvement in computer capabilities . . . or, instead, on a process that qualifies as an 'abstract idea' for which computers are invoked merely as a tool"). But there Netgear runs into a problem: there is nothing in the record that clearly supports this assertion. In making its "generic"/"conventional" argument, Netgear cites to a portion of column 13 of the specification and states that: (1) "media processing units" are "conventional microprocessors capable of 'executing one complex 32 bit instruction per clock cycle'"; and (2) the '434 patent "acknowledges that [a media processing unit is not] 'key' to the alleged invention." (D.I. 51 at 7 (citing '434 patent, col. 13:4-7)) But the cited portion of column 13 does not say this at all. There, the specification is *not* acknowledging that the referenced media processing units are "conventional"—indeed, the word "conventional" is never used. To the contrary, the media processing units are described therein as the "heart" of the claimed architecture. ('434 patent, col. 13:4-5) And otherwise, this portion of the specification simply notes the speed at which these units are capable of operating (i.e., one complex 32 bit instruction per clock cycle), nothing more.[3] While it is not disputed that the media processing units employ "conventional execution units" (i.e., the multiplier, the arithmetic unit, the arithmetic logic unit and the bit manipulation unit), (D.I. 57 at 12), there is nothing in the record to demonstrate that the *claimed arrangement* of these units—e.g., to form media processing units

[3] (*See* D.I. 57 at 11 (Plaintiff noting that "Defendant simply states that a media processing unit can execute 'one complex 32 bit instruction per clock cycle,' which only refers to the speed of operations, not the circuit architecture"))

that can be run concurrently—was well-known and conventional in the prior art. (*Id.* at 12; *see also id.* at 19)[4]

At other points in its briefing, Netgear argues that claim 1 "contains no specific configuration of computer components whatsoever[.]" (D.I. 51 at 11; D.I. 58 at 6) But this assertion seems to be contradicted by another statement Netgear made in its opening brief, where it acknowledged that the "focus" of the claim was on "the concept of processing data by *configuring circuits using a method different from prior art methods*[.]" (D.I. 51 at 12 (emphasis added)) Netgear's prior acknowledgement suggests that claim 1 *does* require at least some sort of configuration of circuit architecture different than what was used in the prior art. And indeed, claim 1 does have certain requirements regarding the components that make up this data processing apparatus. The claim requires that the execution units that are part of the media processing unit each have data inputs, instruction inputs, and data outputs all coupled to the media processing unit input/output and that certain execution units are capable of operating concurrently with certain other execution units. (*See* '434 patent, col. 56:10-12, 17-20; *see also id.*, col. 24:38-40) It also requires that the inputs and outputs of the media processing units be coupled to at least one of the addressable memory input/outputs, such that the media processing

[4] One related challenge in the Section 101 analysis here is that the patent describes the "key element behind the architecture of the [claimed apparatus as] one of re-configurability and re-usability." ('434 patent, col. 13:26-27) Netgear asserts in its briefing that it is not the claimed media processing units or the way they are connected to other components described in the claim that "confers the purported 're-configurability and re-usability'"; instead, Netgear argues that "unclaimed and undisclosed software running on otherwise generic computer components" is what does so. (D.I. 51 at 7) The difficulty for Netgear is that it does not cite to anything in support of this proposition. And the record does not make it clear enough that some unclaimed software component (as opposed to what is described in the claim) is what is the key to delivering the desired re-configurability and re-usability. Indeed, as noted above, the patent at times appears to suggest that the claimed components are in fact key to this outcome. (*See* D.I. 57 at 14 ("Claim 1 is a new apparatus for implementing systems on chips that enable the user to achieve performance of fixed-function implementations at a lower cost."))

units can simultaneously receive instructions and data from the memory, process the data and output results. (*See id.*, cols. 4:28-37, 55:27-30; *see also* D.I. 57 at 12, 14-15)

In sum, based on the record before the Court, Netgear's step one arguments are not well taken. The patent indicates that claim 1 is not simply directed to the generic concept of "data processing" writ large. Instead, it is directed to an apparatus that requires particular components that are configured in a particular way—an apparatus that the patent says helps improve the way computers work. As a result, Netgear's Motion must fail. *See, e.g.*, *Visual Memory*, 867 F.3d at 1259-60 (finding that the asserted claims survived step one of *Alice*, where the claims recited a memory system with particular characteristics, and where the specification described multiple benefits that flowed from the improved memory system); *Thales Visionix Inc. v. United States*, 850 F.3d 1343, 1348-49 (Fed. Cir. 2017) (explaining that the use of conventional sensors and a mathematical equation did not render the claims ineligible, where the claims required a particular configuration of the sensors and a particular way of using the resulting raw data that eliminated problems inherent in prior art methods); *Nw. Univ.*, 2021 WL 4711538, at *4-5 (finding that the claims survived step one of *Alice*, where the invention utilized generic components organized in a non-conventional way and where the plaintiff plausibly alleged how the invention improved upon the prior art). In light of this conclusion, the Court need not reach step two of the *Alice* inquiry. *See, e.g.*, *Thales*, 850 F.3d at 1349.[5]

## IV. CONCLUSION

For all of the above reasons, the Court recommends that Netgear's Motion be DENIED.

[5] Although Altair asserts that Netgear "has raised several claim construction issues that must be decided before the Court can rule on" Netgear's Motion, (D.I. 57 at 8-9), the Court agrees with Netgear that its claim construction proposals do not impact the outcome of the Motion, (D.I. 58 at 8-9).

This Report and Recommendation is filed pursuant to 28 U.S.C. § 636(b)(1)(B), Fed. R. Civ. P. 72(b)(1), and D. Del. LR 72.1. The parties may serve and file specific written objections within fourteen (14) days after being served with a copy of this Report and Recommendation. Fed. R. Civ. P. 72(b)(2). The failure of a party to object to legal conclusions may result in the loss of the right to *de novo* review in the district court. *See Sincavage v. Barnhart*, 171 F. App'x 924, 925 n.1 (3d Cir. 2006); *Henderson v. Carlson*, 812 F.2d 874, 878-79 (3d Cir. 1987).

The parties are directed to the Court's Standing Order for Objections Filed Under Fed. R. Civ. P. 72, dated October 9, 2013, a copy of which is available on the District Court's website, located at http://www.ded.uscourts.gov.

Dated: December 6, 2021

Christopher J. Burke

Christopher J. Burke
UNITED STATES MAGISTRATE JUDGE